

XE1205

433 MHz / 868 MHz / 915 MHz

Low-Power, Integrated UHF Transceiver

GENERAL DESCRIPTION

The XE1205 is an integrated transceiver operating in the 433, 868 and 915 MHz license-free ISM (Industry Scientific and Medical) frequency bands. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The XE1205 offers the unique advantage of narrow-band and wide-band communication, this without the need to modify the number or parameters of the external components. The XE1205 is optimized for low power consumption while offering high RF output power and channelized operation suited for both the European (ETSI EN 300-220-1) and the North American (FCC part 15) regulatory standards. TrueRF™ technology enables a low-cost external component count (elimination of the SAW filter) whilst still satisfying ETSI and FCC regulations.

APPLICATIONS

- Narrow-band and wide-band security systems
- Voice and data over an RF link
- Process and building control
- Access control
- Home automation
- Home appliances interconnection

KEY PRODUCT FEATURES

- Programmable RF output power: up to +15 dBm
- High reception sensitivity: down to -121 dBm at 1.2 kbit/s, -116 dBm at 4.8 kbit/s
- Low power consumption: RX=14 mA; TX = 62 mA @ 15 dBm output power
- Supply voltage down to 2.4V
- Wide band operation: 400 kHz channels for data rates up to 152.3 kbit/s, NRZ coding
- Narrow band operation: 25 kHz channels for data rates up to 4.8 kbit/s, NRZ coding; optional transmitter pre-filtering to enable adjacent channel power below -37 dBm at 25 kHz
- On-chip frequency synthesizer with minimum frequency resolution of 500 Hz
- Continuous phase 2-level FSK modulation
- Incoming data pattern recognition
- Built-in Bit-Synchronizer for incoming data and clock synchronization and recovery
- RSSI (Received Signal Strength Indicator)
- FEI (Frequency Error Indicator)
- 16-byte FIFO for transmit / receive data buffering and transfer via SPI bus

ORDERING INFORMATION

Part number	Temperature range	Package
XE1205I074TRLF	-40 °C to +85 °C	Lead Free VQFN48

TABLE OF CONTENTS

1	Non-Conformance.....	3
2	Functional Block Diagram.....	3
3	Pin Description.....	4
4	Electrical Characteristics	5
4.1	Absolute Maximum Operating Ranges	5
4.2	Specifications	5
4.2.1	Operating Range.....	5
4.2.2	Electrical Specifications	5
5	Description	7
5.1	Data Operation Modes	7
5.2	Receiver Section	7
5.2.1	LNA & Receiver Modes.....	8
5.2.2	Interrupt Signal Mapping.....	8
5.2.3	Receiver in Continuous mode.....	8
5.2.4	Receiver in Buffered Mode	13
5.2.5	DATA pin in Bidirectional or Unidirectional Mode.....	16
5.2.6	Additional Narrow Filter Bandwidths.....	17
5.3	Transmitter Section.....	18
5.3.1	Output Power	18
5.3.2	Transmitter In Continuous Mode.....	18
5.3.3	Transmitter In Buffered Mode.....	20
5.4	Frequency Synthesizer	21
5.4.1	Clock Output For An External Processor.....	21
6	Serial Interface Definition And Principle Of Operation	22
6.1	Serial Control Interface	22
6.1.1	Chip Configuration Via SPI_CONFIG Interface	23
6.1.2	Data Transmission And Reception Via SPI_DATA Interface	25
6.2	Configuration And Status Registers.....	26
6.2.1	Configuration Register: General Description	26
6.2.2	Mcpam Configuration Register (Main Configuration Parameters).....	27
6.2.3	Irqparam Configuration Register (IRQ Parameters).....	28
6.2.4	Txparam Configuration Register (Transmitter Configuration Parameters).....	29
6.2.5	Rxparam Configuration Register (Receiver Configuration Parameters).....	29
6.2.6	Pattern Register	31
6.2.7	Oscparam Configuration Register (Oscillator Parameters)	32
6.2.8	Tparam Configuration Register (Test And Special Settings).....	33
6.3	Operating Modes	34
6.3.1	XE1205 Switching Time Using SPI_CONFIG Interface	34
6.3.2	XE1205 Switching Time Using SW(1:0) Pins	36
6.4	Selection Of The Reference Frequency	36
6.5	Clock Output Interface	37
6.6	Default Settings At Power-Up	37
6.7	Pad Configuration Versus Chip Modes.....	37
7	Application Information.....	39
7.1	Matching Network Of The Receiver	39
7.2	Matching Network Of The Transmitter	39
7.3	VCO Tank	42
7.4	Loop Filter Of The Frequency Synthesizer	43
7.5	Reference Crystal For The Frequency Synthesizer	44
8	Packaging Information	45

The XE1205 single-chip solution is an integrated circuit intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with non-return to zero data coding. The device is available in a VQFN 48 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 433 MHz and 868 MHz European bands and the North American 902-928 MHz ISM band. The single chip transceiver operates down to 2.4V. Its ability to operate with 25 kHz channel spacing makes it compliant with requirements of ETSI EN300 220-1 and makes the XE1205 ideal for automatic meter reading and alarms.

1 NON-CONFORMANCE

Please note the products whose date-codes start with N4K and N5K (except N5K3760 and N5K3760A) exhibit a non-conformance to specification. The non-conformance affects the FIFO buffer described in section 5.2.4. Please use the FIFO in this product only in conjunction with the Technical Note TN1205.01 (available from the XEMICS web site). All other date-codes are in conformance with the specification.

2 FUNCTIONAL BLOCK DIAGRAM

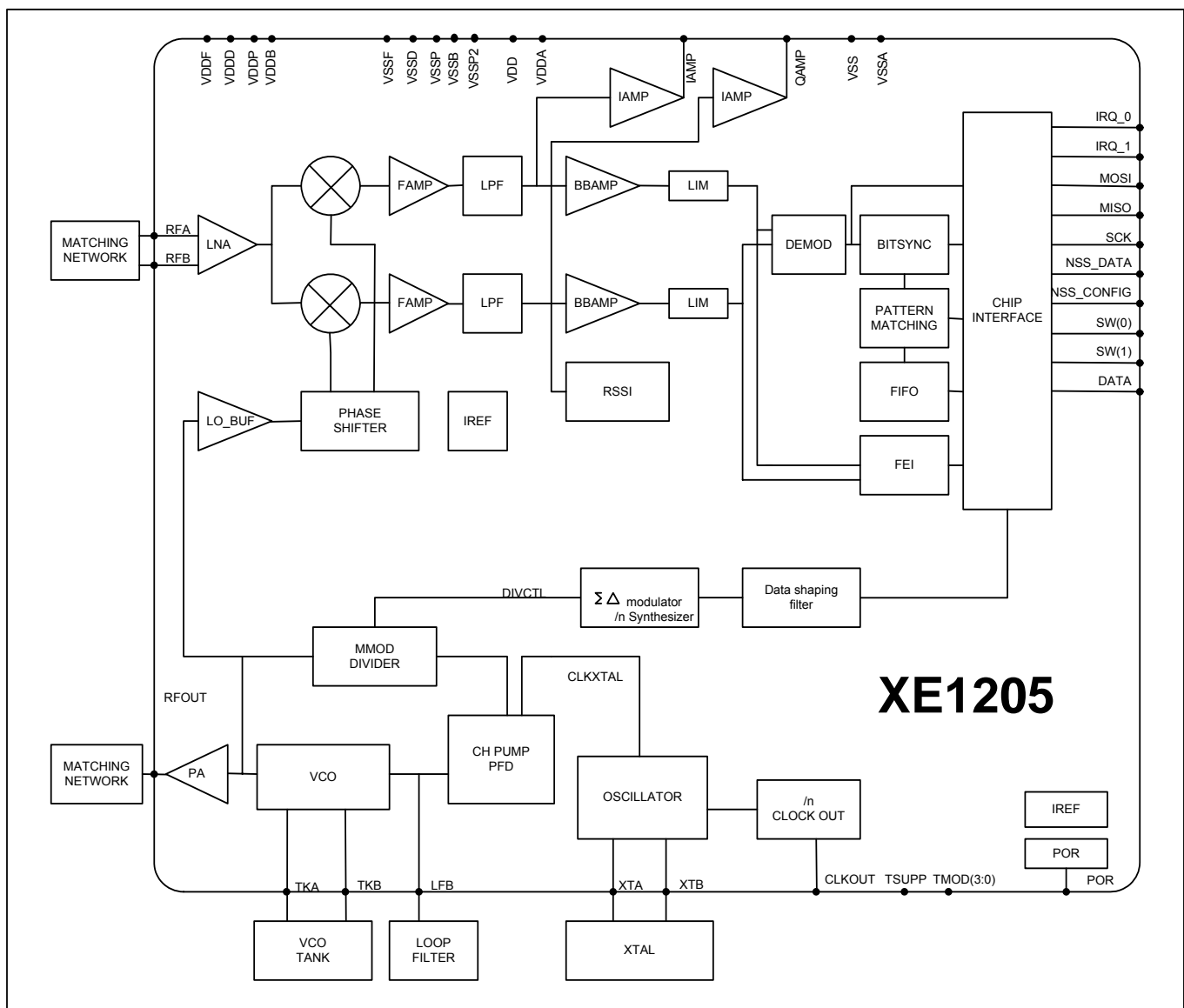


Figure 1: XE1205 block diagram.

3 PIN DESCRIPTION

PIN	NAME		DESCRIPTION
1	SW(0)	I/O	Transmit/Receive/Stand-by/Sleep Mode Select
2	SW(1)	I/O	Transmit/Receive/Stand-by/Sleep Mode Select
3	NC		Not connected (should be grounded)
4	NC		Not connected (should be grounded)
5	RFA	I	RF Input
6	RFB	I	RF Input
7	VSSP2		Power Amplifier Ground
8	VSSP2		Power Amplifier Ground
9	RFOUT	O	RF Output
10	VDDP		Power Amplifier Supply Voltage
11	VSSP		Power Amplifier Ground
12	VDDF		Second HF Analog Supply voltage
13	VSSF		Second HF Analog Ground
14	TKA	I/O	VCO Tank
15	VSSF		Second HF Analog Ground
16	TKB	I/O	VCO Tank
17	VSSF		Second HF Analog Ground
18	LFB	I/O	PLL Loop Filter
19	VDDD		HF Digital Supply Voltage
20	VSS		LF Digital Ground
21	NSS_CONFIG	I	SPI SELECT CONFIG
22	NSS_DATA	I	SPI SELECT DATA / DATAIN
23	VDD		LF Digital Supply Voltage
24	IRQ_0	O	Interrupt (PATTERN/FIFOEMPTY)
25	IRQ_1	O	Interrupt(DCLK/FIFOFULL)
26	DATA	I/O	Data
27	CLKOUT	O	Output clock at reference frequency divided by 2, 4, 8, 16, 32
28	MISO	O	SPI Master Input Slave Output
29	MOSI	I	SPI Master Output Slave Input
30	SCK	I	SPI CLOCK
31	XTA	I/O	Ref Xtal / Input of external clock
32	VSSA		LF analog ground
33	XTB	I/O	Reference Xtal
34	VDDA		LF Analog Supply Voltage
35	POR	I/O	Not used (should not be connected)
36	NC		Not connected (should be grounded)
37	TIBIAS	I/O	(connected to VSS in normal operation)
38	TSUPP		Test Circuit Supply Voltage (connected to VSS in normal operation)
39	VDDA		LF Analog Supply Voltage
40	VSSA		LF analog ground
41	QAMP	O	Output of Q low-pass filter
42	IAMP	O	Output of I low-pass filter
43	TMOD(3)	I/O	(connected to VSS in normal operation)
44	TMOD(2)	I/O	(connected to VSS in normal operation)
45	TMOD(1)	I/O	(connected to VSS in normal operation)
46	TMOD(0)	I/O	(connected to VSS in normal operation)
47	NC		Not connected (should be grounded)
48	NC		Not connected (should be grounded)

Table 1: Pin description

4 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM OPERATING RANGES

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmax	Supply voltage	-0.5	3.9	V
Tmr	Storage temperature	-55	125	°C
ML	Receiver input level		-5	dBm

Table 2: Absolute Maximum Operation Ranges

The device is ESD sensitive and should be handled with precaution.

4.2 SPECIFICATIONS

4.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDDop	Supply voltage	2.4	3.6	V
Trop	Temperature	-40	85	°C
Clop	Load capacitance on digital ports	-	25	pF

Table 3: Operating Range

4.2.2 Electrical Specifications

The table below gives the electrical specifications of the transceiver under the following conditions:

Supply Voltage = 3.3V, temperature = 25 °C, 2-level FSK without pre-filtering, $f_c = 915$ MHz, $\Delta f = 5$ kHz, Bit rate = 4.8 kbit/s, $BW_{SSB} = 10$ kHz, BER = 0.1% (at the output of the bit synchronizer), matched impedances, environment as defined in section 6, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	uA
IDDST	Supply current in standby mode	Quartz oscillator (39 MHz) enabled	-	0.85	1.10	mA
IDDR	Supply current in receiver mode		-	14	16.5	mA
IDDT	Supply current in transmitter mode	RFOP = 5 dBm	-	33	40	mA
		RFOP = 15 dBm	-	62	75	mA
RFS	RF sensitivity	A-mode	-	-116	-113	dBm
		B-mode	-	-102	-99	dBm
RFS_12	RF sensitivity at 1.2 kb/s	A-mode	-	-121	-118	dBm
		B-mode	-	-107	-104	dBm
FDA	Frequency deviation	Programmable	1	-	255	kHz
CCR	Co-channel rejection		-13	-10	-	dBc
IIP3	Input intercept point (from LNA input to base-band filter output)	$funw = f_{LO} + 1$ MHz and $f_{LO} + 1.995$ MHz				
		A-mode	-37	-33	-	dBm
		B-mode	-21	-18	-	dBm
BW	Base band filter bandwidth (SSB)	Programmable (1)	-	10	-	kHz
			-	20	-	kHz
			-	40	-	kHz
			-	200	-	kHz

WIRELESS AND SENSING PRODUCTS

Symbol	Description	Conditions	Min	Typ	Max	Unit
ACR_25	Receiver adjacent channel rejection ratio at 25 kHz	funw = $f_{LO} + 25$ kHz single tone Pw=-110 dBm, A-mode BW (SSB) = 10 kHz BW (SSB) = 8 kHz (2)	17 27	20 30	- -	dBc dBc
ACR_50	Receiver adjacent channel rejection ratio at 50 kHz	funw = $f_{LO} + 50$ kHz single tone Pw=-110 dBm, A-mode	37	40	-	dBc
BR	Bit rate	Programmable	1.2	-	152.3	kbit/s
RFOP	RF output power	Programmable RFOP1 RFOP2 RFOP3 RFOP4	-3 +2 +7 +12	0 +5 +10 +15	- - - -	dBm dBm dBm dBm
ACP	Transmitter adjacent channel power (measured at 25 kHz offset)	Pre-filter enabled (RFOP3 mode) Measurement conditions as defined by EN 300 220-1 V1.3.	-	-	-37	dBm
FR	Synthesizer frequency range	Programmable	433 863 902	- - -	435 870 928	MHz MHz MHz
TS_SRE	Receiver wake-up time	Quartz oscillator enabled	-	700	850	us
TS_STR	Transmitter wake-up time	Quartz oscillator enabled	-	250	350	us
TS_FS	Frequency synthesizer wake-up time	Quartz oscillator enabled	-	200	250	us
TS_RE	Receiver wake-up time	Frequency synthesizer enabled	-	500	600	us
TS_TR	Transmitter wake-up time	Frequency synthesizer enabled	-	100	150	us
TS_RFSW	Receiver recovery time when switch between 2 channels	Between 2 channels at 1 MHz from each other	-	tbd	tbd	us
TS_TFSW	Transmitter recovery time when switching between 2 channels	Between 2 channels at 1 MHz from each other	-	150	250	us
TS_RSSI	RSSI wake-up time	Receiver enabled	-	-	1.5	ms
TS_OS	Quartz oscillator wake-up time	Fundamental 3 rd overtone	- -	1 7	2 -	ms ms
TS_FEI	FEI wake-up time	Receiver enabled	-	2/BR	-	ms
XTAL	Quartz oscillator frequency	Fundamental or third harmonic	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77'824	-	500	-	Hz
VTNR	Equivalent input thresholds of the RSSI	A-mode, low range:VTNR1 VTNR2 VTNR3 A-mode, high range:VTNR1 VTNR2 VTNR3	- - - - - -	-110 -105 -100 -95 -90 -85	- - - - - -	dBm dBm dBm dBm dBm dBm
SPR	Spurious emission in receiver mode	(3)	-	-65	-	dBm
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%
VOH	Digital output level high	% VDD	75	-	-	%
VOL	Digital output level low	% VDD	-	-	25	%

Table 4: Electrical Specifications

- (1) Additional bandwidths can be selected with special settings described in section 5.2.8.
- (2) With special settings as described in sections 4.2.6 and 5.2.8.
- (3) SPR strongly depends on the design of the application board and the choice of the external components. Values down to -70 dBm can be achieved with careful design.

5 DESCRIPTION

The XE1205 is a direct conversion (Zero-IF) half-duplex data transceiver. It includes receiver, transmitter, frequency synthesizer and control logic. The circuit is intended for operation in the following three frequency bands 433 MHz, 868 MHz, and 915 MHz and uses 2-level FSK modulation.

The XE1205 is programmed by a microcontroller through the 3-wire fully-compatible SPI serial bus (MOSI, MISO, SCK) to write to and read from the configuration registers.

The circuit consists of 4 main functional blocks:

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver comprises a low-noise amplifier, down-conversion mixers, baseband filters, baseband amplifiers, limiters, demodulator and bit synchronizer. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream DATAOUT and synchronized clock DCLK. This may be easily used to sample the DATAOUT signal with minimal external processor overhead. In addition, the receiver includes a Received Signal Strength Indicator (RSSI) function and a Frequency Error Indicator (FEI) function that provides an indication of the local oscillator frequency error. A pattern recognition function may be used to detect a user-programmable reference word in the incoming bit stream. The bandwidth of the base-band filters, the frequency deviation of the expected incoming FSK signal as well as the bit rate of the received data signal are all user-programmable.

The transmitter performs the modulation of the carrier by an input baseband data signal and the transmission of the modulated signal. The frequency synthesizer is modulated directly. The modulated signal is then amplified by the on-chip RF power amplifier. The output power is user-programmable to one of four possible values. The frequency deviation and the bit rate for the transmit signal are the same as those programmed for the receiver section. User-defined pre-filtering should be enabled to ensure compliance with the requirements of ETSI EN 300 220-1 regarding transmission at 25 kHz channel spacing.

The frequency synthesizer generates the local oscillator (LO) signal for the receiver section as well as the FSK modulated signal for the transmitter section. The core of the synthesizer is implemented with a PLL structure. The frequency is user-programmable with a minimum frequency resolution of 500 Hz in the 3 frequency bands, 433 MHz, 868 MHz and 915 MHz. This section includes a crystal oscillator whose signal is the reference for the PLL. This reference frequency is divided by 2, 4, 8, 16, or 32 and is made available at the CLKOUT pin to serve as a clock signal for an external processor.

The control block generates the control signals according to the setting in its set of configuration registers.

The service block performs all the necessary functions for the circuit to work properly, including the internal voltage and current sources.

5.1 DATA OPERATION MODES

The XE1205 is user-programmable between two modes of operation:

Continuous mode: each bit transmitted or received is accessed directly at the DATA input/output pin.

Buffered mode: a 16-byte FIFO is used to store each data byte transmitted or received. This data is written to/read from the FIFO via the SPI bus. It reduces processor overhead and reduces connections (the DATA input/output pin is not used in this operation mode)

5.2 RECEIVER SECTION

The XE1205 is set to receive mode when MCPParam_Select_mode is low by setting MCPParam_Chip_mode(1:0) to "01". If MCPParam_Select_mode is high the XE1205 is set to receive mode by setting SW(1:0) to "01".

5.2.1 LNA & Receiver modes

The LNA of the receiver has two programmable operation modes: the high sensitivity mode, Mode A, for reception of weak signals; and the high linearity mode, Mode B, for strong signals. The operation mode is defined by the value of the Rmode bit in RXParam_Rmode configuration register.

Mode A: High sensitivity mode, approximately 13dB better than in Mode B (see 4.2.2, RFS parameter)

Mode B: High Linearity mode, IIP3 approximately 15dB higher than in Mode A (see 4.2.2, IIP3 parameter)

5.2.2 Interrupt Signal Mapping.

In receiver mode, two lines are dedicated to interrupt information. The interrupt pins are IRQ_0 and IRQ_1. IRQ_0 has 3 selectable sources. IRQ_1 has 2 selectable sources. The two following tables summarize the interrupt management.

IRQParam_RX_irq_0	MCPParam_Buffered_mode	IRQ_0	IRQ_0 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Write_byte
10	1	Output	/fifoempty
11	1	Output	Pattern
00	0	Output	Pattern
01	0	Output	RSSI_irq
10	0	Output	Pattern
11	0	Output	Pattern

Table 5: IRQ_0 interrupt sources in receive mode.

IRQParam_RX_irq_1	MCPParam_Buffered_mode	IRQ_1	IRQ_1 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Fifofull
10	1	Output	RSSI_irq
11	1	Output	RSSI_irq
00	0	Output	DCLK
01	0	Output	DCLK
10	0	Output	DCLK
11	0	Output	DCLK

Table 6: IRQ_1 interrupt sources in receive mode.

5.2.3 Receiver in Continuous Mode

In this mode, the receiver has two output signals indicating recovered clock, DCLK and recovered NRZ bit DATA. DCLK is connected to output pin IRQ_1 and DATA is connected to pin DATA configured in output mode. The bit synchronizer controls the recovered clock signal, DCLK. If the bit synchronizer is enabled by setting the bit /RXParam_Disable_bitsync to "0" (default value), the clock recovered from the incoming data stream appears at DCLK.

If the bit synchronizer is disabled, the DCLK output is held low and the demodulator output appears at DATA. The function of the bit synchronizer is to remove glitches from the data stream and to provide a synchronous clock at DCLK. The output DATA is valid at the rising edge of DCLK. The following diagram shows the receiver chain operating in this mode.

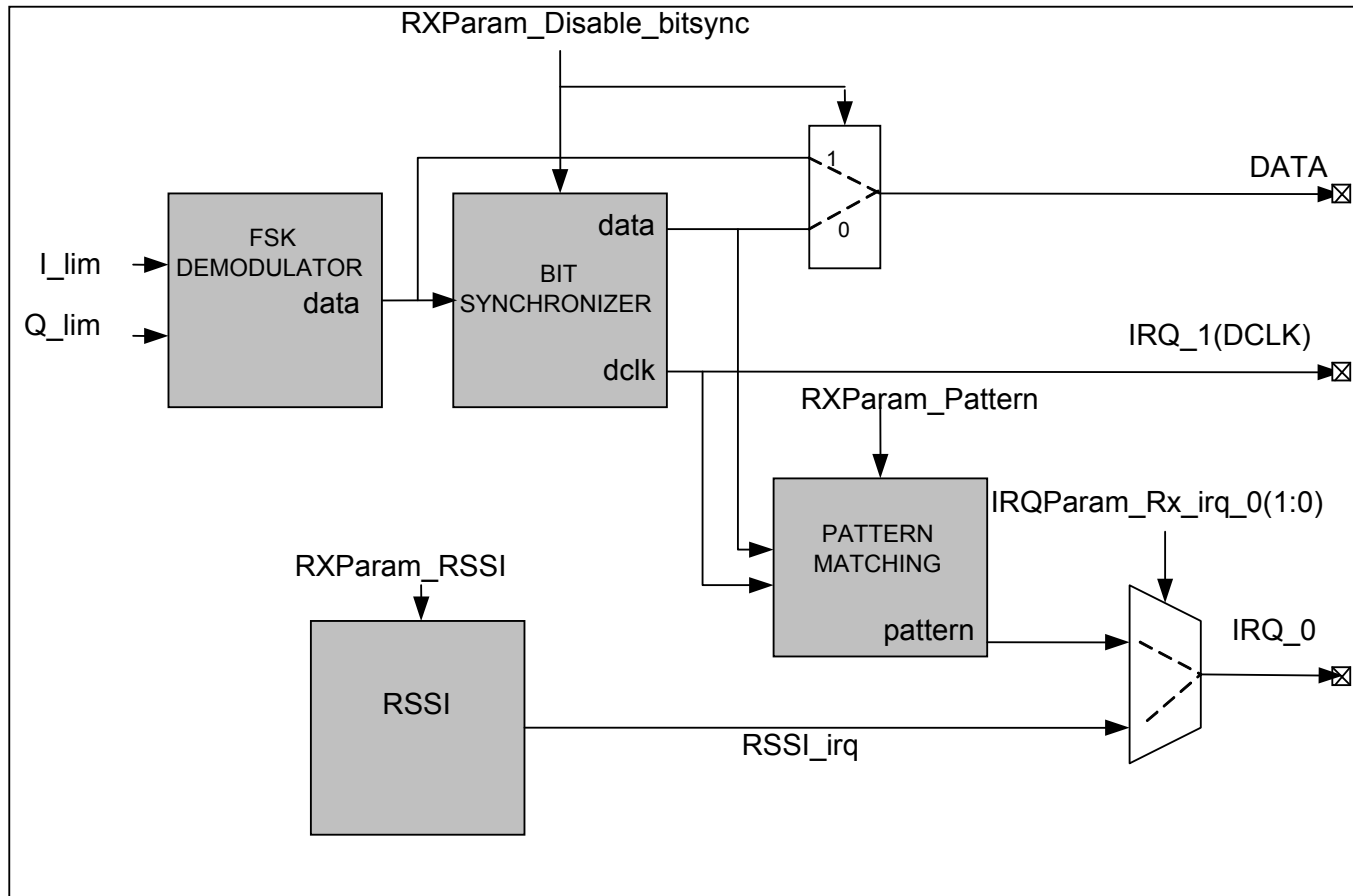


Figure 2: Receiver chain in continuous mode

5.2.3.1 Demodulator in Continuous Mode

The demodulator section comprises FSK demodulator, bit synchronizer, and Pattern Recognition blocks.

Data from the FSK baseband limited signals I_lim and Q_lim is first demodulated before passing to the bit synchronizer.

If the end-user application requires direct access to the output of the demodulator, then the $RXParam_Disable_bitsync$ bit is set high. In this case the demodulator output is directly connected to the DATA pin and the IRQ_1 pin (DCLK) is set to low.

For proper operation of the demodulator the modulation index β of the input signal should meet the following condition:

$$\beta = \frac{2\Delta f}{BR} \geq 2$$

where Δf is the frequency deviation and BR the bit rate.

5.2.3.2 Bit Synchronizer In Continuous Mode

The raw output signal from the demodulator may contain jitter and glitches. The bit synchronizer converts the data output of the demodulator into a glitch-free bit-stream DATA and generates a synchronized clock DCLK to be used for sampling the DATA output (see below). DCLK is available on pin IRQ_1 when the chip operates in continuous mode.

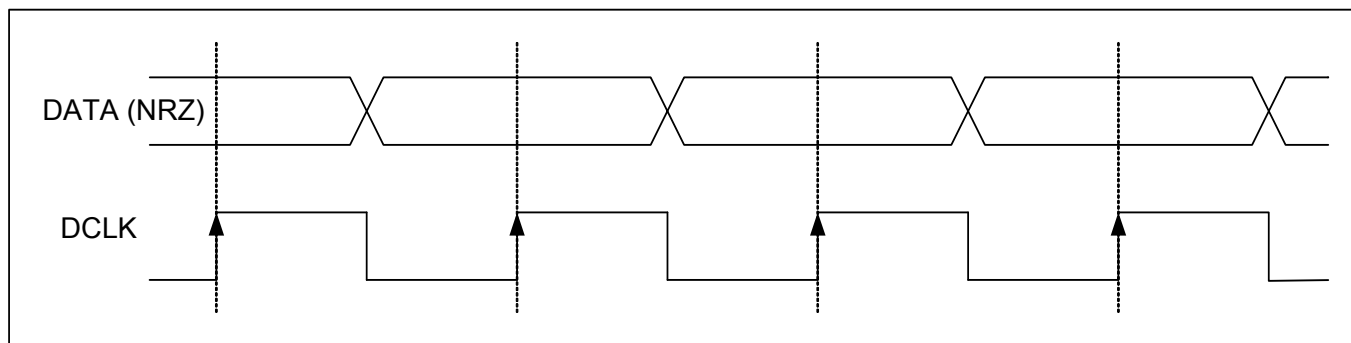


Figure 3: Bit synchronizer timing diagram

To ensure the correct operation of the bit synchronizer, in addition to the requirement for the modulation index defined in Section 5.2.3.1, the following conditions have to be satisfied:

- A preamble of 24 bits is required for synchronization
- The preamble must be a sequence of '0' and '1' sent alternatively
- The bit stream must have at least one transition from '0' to '1' or from '1' to '0' every 8 bits during data transmission
- The bit rate accuracy must be better than 5% (3% for Konnex mode operation)

The bit synchronizer is enabled by default. It is controlled by `RXParam_Disable_bitsync`. If the bit synchroniser is disabled the output of the demodulator is directed to DATA and the DCLK output (IRQ_1 Pin in continuous mode) is set to '0'.

The received bit rate is defined by the value of the `MCPParam_Br(6:0)` configuration register, and is calculated as follows:

$$\text{Bit rate} = \frac{152.34e3}{\text{int}(\text{Br}(6:0)) + 1}$$

Where `int(x)` is the integer value of the unsigned binary representation of `x`.

Note: For the Konnex standard operation, the bit rate is fixed at 32.7 kbit/s. The bit synchronizer is automatically configured with the right bit rate value if the `MCPParam_Knx` configuration bit is set high.

5.2.3.3 Pattern Recognition Block In Continuous Mode

In receive mode this feature is activated by setting the `RXParam_Pattern` configuration register bit to high. The demodulated signal is compared with a pattern stored in the `Reg_pattern(31:0)` registers. The PATTERN signal (mapped to output pin IRQ_0) is driven by the output of this comparator and is synchronized by DCLK. It is set to high when a matching condition is detected, otherwise set to low. PATTERN output is updated at the rising edge of DCLK. The number of bits used for comparison is defined in the `RXParam_Psize(1:0)` register and the number of tolerated errors for the pattern recognition is defined in the `RXParam_Ptol(1:0)` register. Figure 4, below, illustrates the pattern matching process.

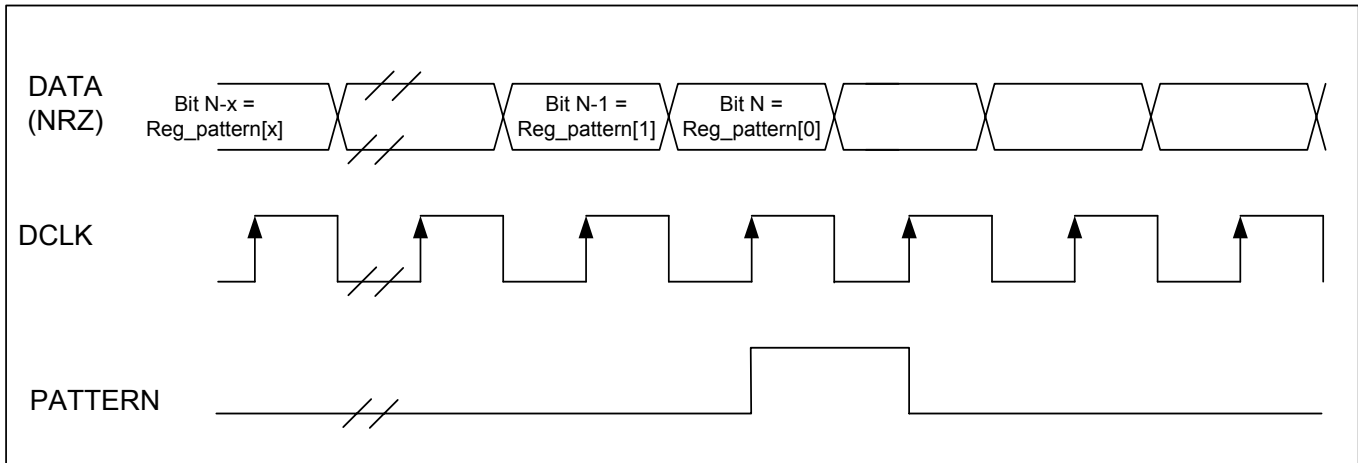


Figure 4: Pattern matching operation.

Note: The pattern recognizer is available only if the bit synchronizer is working.

5.2.3.4 RSSI in Continuous Mode

This function provides a Received Signal Strength Indication based on the signal level at the output of the base-band filter. To activate this function, the bit `RXParam_RSSI` must be set to “1”. When activated, the 2-bit status information is stored in register `RXPARAM_RSSI_OUT(1:0)` and may be read through the serial control interface. The meaning of this status information is given in the table below, where V_{RFFIL} is the differential amplitude of the equivalent input RF signal when the receiver is operated in A-mode. The thresholds $VTHR_i$ are at the output of the base-band filter divided by the gain between the input of the receiver and this output.

<code>RXPARAM_RSSI_out(1:0)</code>	Description
0 0	$V_{RFFIL} \leq VTHR1$
0 1	$VTHR1 < V_{RFFIL} \leq VTHR2$
1 0	$VTHR2 < V_{RFFIL} \leq VTHR3$
1 1	$VTHR3 < V_{RFFIL}$

Table 7: RSSI status description

The operating range of the RSSI measurement may be changed by programming the `RXParam_RSSI_range` bit; in this way two ranges with three $VTHR_i$ values may be selected. The time diagram of an RSSI measurement is given in Figure 5. When the RSSI function has been activated the signal strength is periodically measured and the result is stored in `RSSI_out_int`; this result is transferred to the register `RXParam_RSSI_out(1:0)` each time this register is read via the SPI interface. `TS_RSSI` is the wake-up time required after the function has been activated to get a valid result and its value is given in section 3.2.2. `TS_RSSIM` is the period between two successive measurements and its value depends on the selected frequency deviation (100 μs for $\Delta f > 20$ kHz, 200 μs for 10 kHz $< \Delta f \leq 20$ kHz, 300 μs for 7 kHz $< \Delta f \leq 10$ kHz, 400 μs for 5 kHz $< \Delta f \leq 7$ kHz, and 500 μs $\Delta f \leq 5$ kHz).

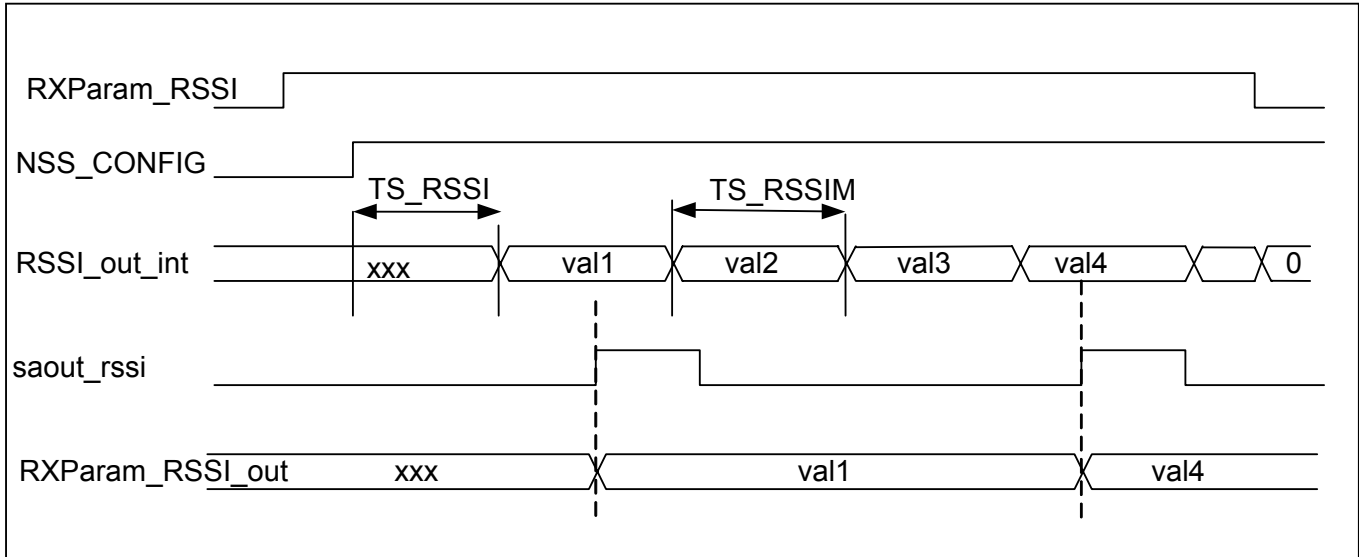


Figure 5: RSSI measurement timing diagram

Saout_rssi is internally generated during a read sequence of RXParam_RSSI_out register.

The RSSI block can also be used in interrupt mode by setting the bit IRQParam_RSSI_int to 1. When RSSI_out_int is equal or greater than a predefined value stored in IRQParam_RSSI_thr(1:0), the signal IRQParam_RSSI_signal_detect (can be read in the Configuration register) goes high and an interrupt signal RSSI_irq is generated. This interrupt signal can be used by a microcontroller if IRQParam_RX_irq_1 is set to "10" or "11" (see table 1). The interrupt is cleared by writing a 1 to the bit IRQParam_RSSI_signal_detect. If the bit IRQParam_RSSI_int remains high, the process starts again. The next figure shows the timing diagram of RSSI in interrupt mode.

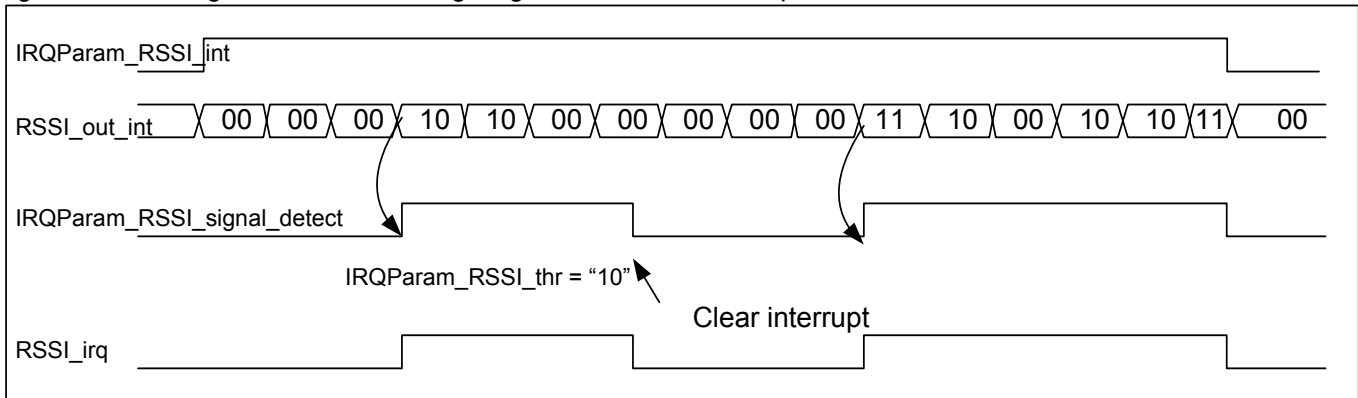


Figure 6: RSSI generating interrupt signal when detecting a threshold

5.2.3.5 Frequency Error Indicator in Continuous Mode – FEI

The block is switched ON by writing bit RXParam_FEI to '1'. This function provides information about the frequency error of the local oscillator compared with the input carrier frequency and can be used to implement an AFC. The condition on the modulation index for proper behavior of the FEI function is:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

Where Δf is the frequency deviation and BR is the bit rate.

The time diagram of an FEI measurement is given in the next figure. When the FEI block has been woken up and is ready, and as long as the block is kept on, the frequency error is measured and the current result of the measurement is loaded in the register RXParam_FEI_out(15:0) each time register 12 is read. TS_FEI is the time required for the first evaluation to be completed after the block has been started up and its value is given in section 4.2.2. Since the contents of the configuration register is validated at the rising edge of the enable signal NSS_CONFIG, the FEI block is actually started up at this time.

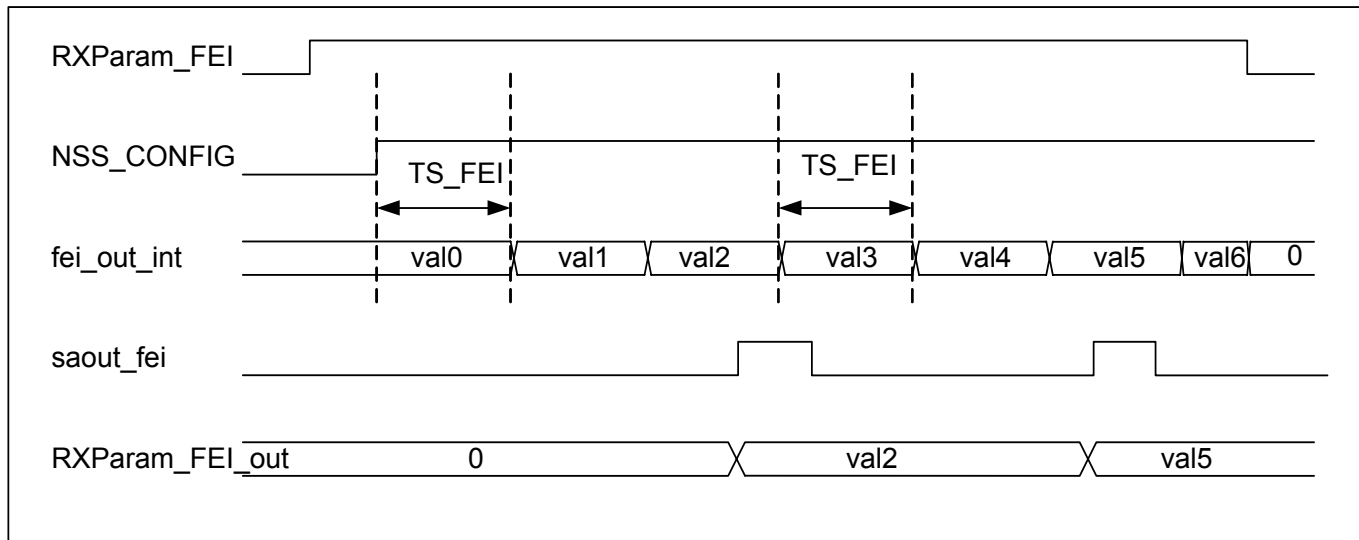


Figure 7: Timing diagram of an FEI measurement

To guarantee proper behavior of the FEI, the operation must be done when a preamble as defined in section 5.2.3.1 is received, and the sum of the frequency offset and the signal bandwidth (single sided) must be lower than the base band filter bandwidth (single sided). That is:

$$F_{\text{offset}} + \text{SignalBW} < \text{FilterBW}.$$

Where f_{offset} is the difference between the carrier frequency and the LO frequency, SignalBW is the signal bandwidth (single side) equal to the sum of the bit rate divided by 2 and the frequency deviation ($\text{BR}/2 + \text{DF}$), and FilterBW is the channel filter bandwidth defined by RXParam_BW(1:0) parameters.

The frequency error can be calculated by the following formula:

$$\text{The frequency error} = 500 \cdot \text{int}(\text{FEI_out}(15:0)) \text{ in Hz}$$

Where $\text{int}(x)$ is the integer value of the signed binary representation of x .

In fact RXParam_FEI_out(15:0) can directly be added to the register MCPParam_Freq_lo(15:0) without further calculation by a microcontroller since the PLL step is 500 Hz i.e. RXParam_FEI_out (15:0) represents the number of step needed to compensate the frequency error .

Saout_fei is internally generated during a read sequence of register 12 in the same way as saout_rssi.

5.2.4 Receiver in Buffered Mode

In this mode, the output of the bit synchronizer, i.e. the demodulated and resynchronized signal and the clock signal DCLK are not sent directly to the output pins DATA and IRQ_1 (DCLK). These signals are used to store the demodulated signal by packet of 8 bits in a 16 bytes FIFO. The following figure shows the receiver chain in this mode.

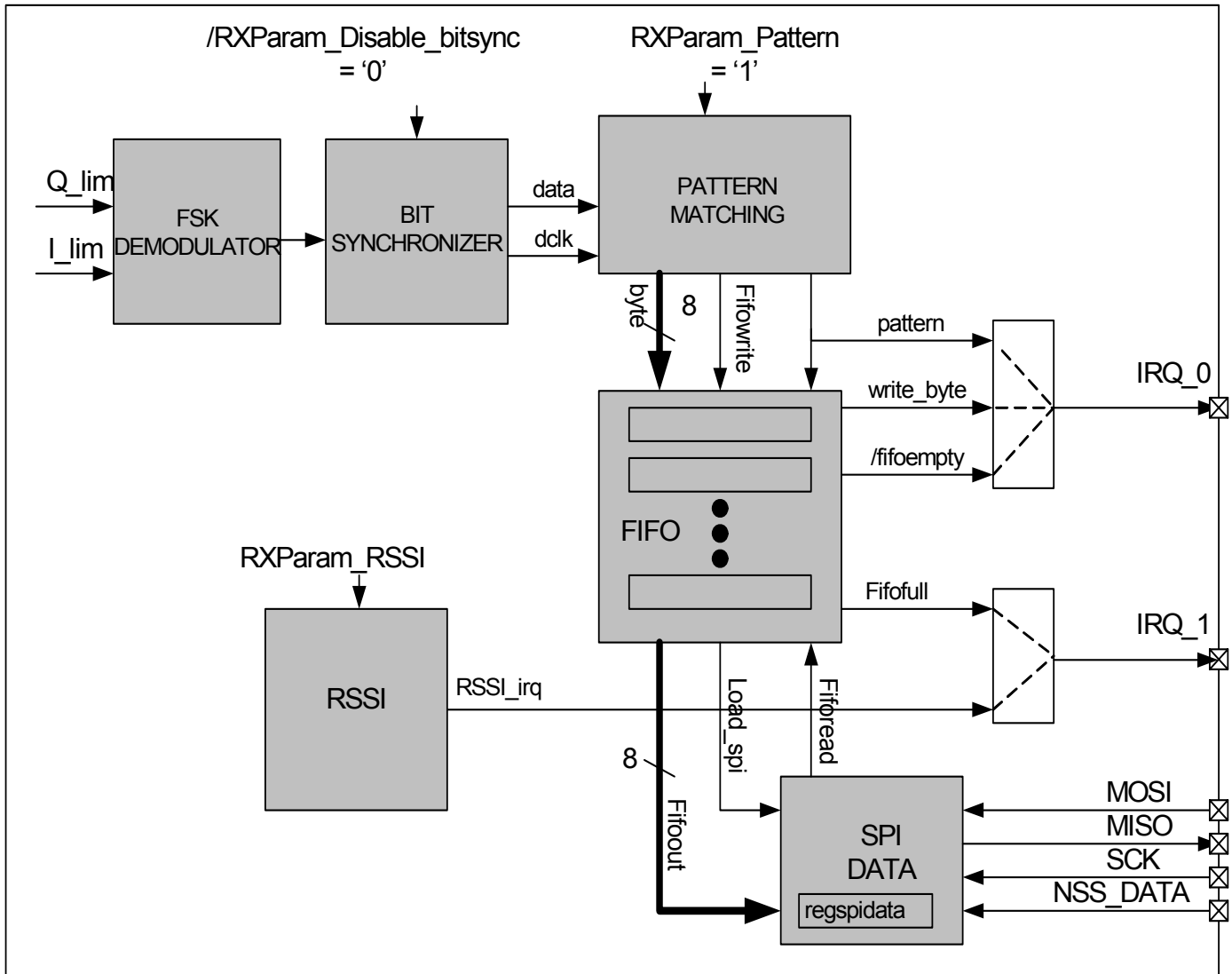


Figure 8: Receiver chain in buffered mode

The FSK demodulator, bit synchronizer and pattern matching block work as described in section 5.2.2 but they are used with two additional blocks, FIFO and SPI.

When the chip is in receive mode and the MCPParam_Buffered_mode bit is set to high then all the blocks described above are enabled. In a normal communication frame the data stream comprises a 24 bit preamble, pattern (refer to section 5.2.3.3) and the data. Upon receipt of a recognized pattern, the receiver recognizes the start of a frame, strips off the preamble and pattern, then transmits the data to the microcontroller. This automated data recovery reduces the overhead for the host controller.

The IRQParam_Start_fill bit determines how the FIFO is filled:

If IRQParam_Start_fill is low, data only fills the FIFO subject to a correct pattern match. Data is shifted into the pattern recognition block which continuously compares the received data with the contents of the Reg_pattern(31:0) configuration register. If a match occurs a start sequence is detected, and the internal output of the pattern matching block is asserted for one bit length and the IRQParam_Start_detect bit is also asserted. This internal signal may be mapped to the IRQ_0 output using interrupt signal mapping (please refer to section 5.2.2). Once a pattern match has occurred, the pattern recognition block will remain inactive until IRQParam_Start_detect is re-asserted.

If IRQParam_Start_fill is high, FIFO filling is initiated by asserting IRQParam_Start_detect.

Once sixteen bytes have been written to the FIFO the IRQParam_Fifofull signal is asserted. Data should then normally be read out. If no action is taken the FIFO will overflow and subsequent data will be lost. If this occurs the IRQParam_Fifooverflow bit is set. The IRQParam_Fifofull signal can be mapped to pin IRQ_1 as an interrupt for a microcontroller if IRQParam_RX_irq_1 is set to "01" (please refer to section 5.2.2).

To recover from an overflow situation a '1' must be written to IRQParam_Fifooverflow; this clears the contents of the FIFO, resets all FIFO status flags and re-initiates pattern matching.

Pattern matching can also be re-initiated during a FIFO filling sequence by writing a '1' to IRQParam_Start_detect.

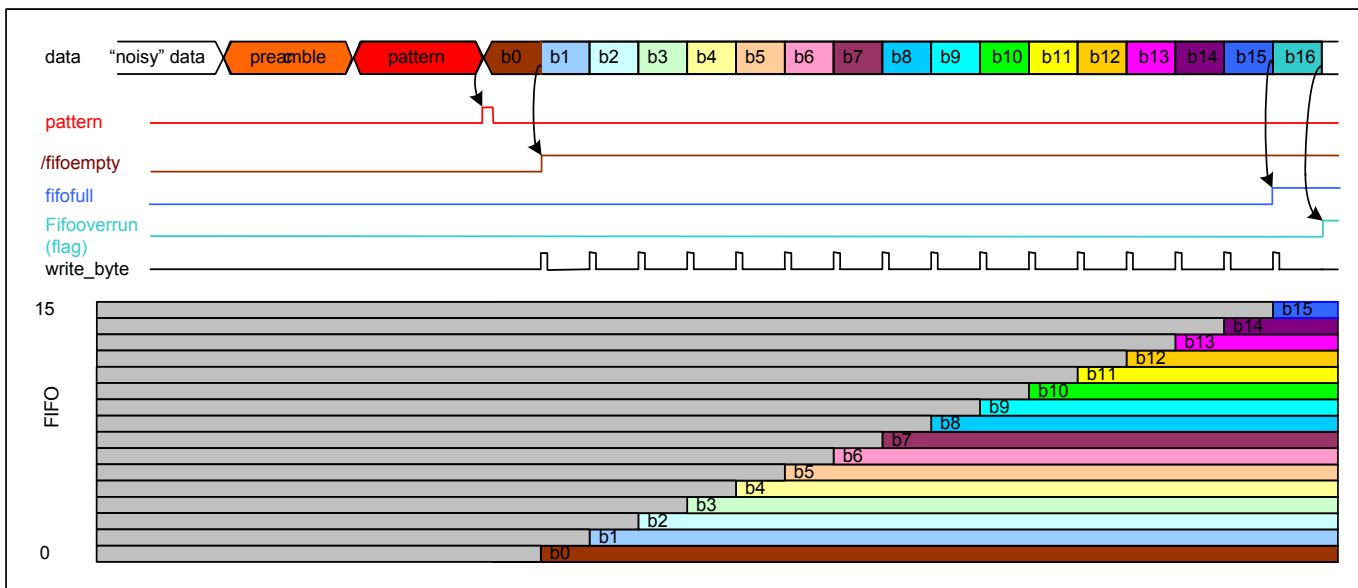


Figure 9: Start detection and FIFO filling

The FIFO filling process is shown in detail in Figure 9. As the first byte is written into the FIFO the signal /fifempty goes high indicating that at least one byte is present. The microcontroller can then read the contents of the FIFO via the SPI interface. Once all data have been read from the FIFO then /fifempty goes low. Once the last bit of the sixteenth byte has been written into the FIFO then the signal Fifofull is asserted; data should be read before the next byte is received. This is described in Figure 10.

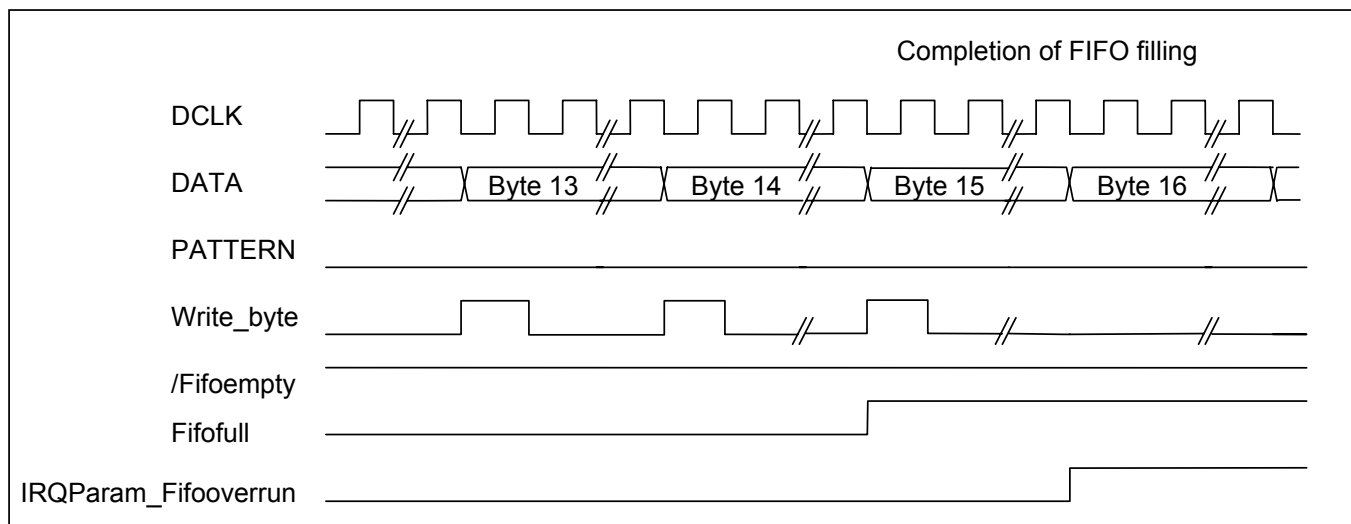


Figure 10: Completion of FIFO filling

The /fifoempty signal can be used as an interrupt signal for a microcontroller by mapping to pin IRQ_0 if IRQParam_RX_irq_0(1:0) is set to "10" (please refer to section 5.2.2). Alternatively, the WRITE_BYTE signal may also be used as an interrupt if IRQParam_RX_irq_0(1:0) is set to "01".

5.2.4.1 Demodulator in Buffered Mode

Demodulation in buffered mode occurs in the same way as in continuous mode (section 5.2.3.1). Received data is directly read from the FIFO and the DATA and DCLK pins are not used.

5.2.4.2 Bit Synchronizer in Buffered Mode

In buffered mode the bit synchronizer is automatically enabled (DCLK is not externally available).

5.2.4.3 Pattern Recognition Block In Buffered Mode

In buffered mode the pattern recognition block is automatically enabled. The PATTERN signal may be mapped to pin IRQ_0. Please refer to section 5.2.2 for further details.

5.2.4.4 RSSI in Buffered Mode

In buffered mode the Received Signal Strength Indication operates the same way as in continuous mode. In buffered mode, however, RSSI_irq may be mapped to IRQ_1 (please refer to section 5.2.2) instead of to IRQ_0 in continuous mode.

5.2.4.5 Frequency Error Indicator in Buffered Mode – FEI

In buffered mode the Frequency Error Indication operates the same way as in continuous mode. Please refer to section 5.2.3.5 for more details.

5.2.5 DATA pin in Bidirectional Or Unidirectional Mode

The DATA pin is bi-directional by default, and is used in both transmit and receive modes. In receive mode, DATA represents demodulated received data. In transmit mode baseband data is applied to this pin.

Some applications may require a separate input and output for transmitted and received data respectively. In this case the MCPParam_Data_unidir configuration register bit must be set to '1'. The DATA pin is then set permanently to an output for received data, and NSS_DATA is used as the input.

5.2.6 Additional Narrow Filter Bandwidths

The lowest bandwidth for the base-band filter which can be selected by changing only a 2-bit word in the configuration register is 10 kHz. However, as described in section 5.2.8, some special settings allow this bandwidth to be further reduced. This option allows the user to improve the selectivity of the receiver for very narrow-band applications. Activating this option is advised for bit rates and frequency deviations not higher than 4.8 kbit/s and 5 kHz and if the LO frequency of the receiver is well controlled, for instance by means of a very accurate crystal or the activation of an AFC. The table below gives the sensitivity and the adjacent channel rejection for BR = 4.8 kbit/s and $\Delta f = 5$ kHz for different bandwidths.

Bandwidth SSB	TParam_Low_BW	TParam_Code_BW(8:0)	Sensitivity RFS (BER=0.1%)	Adjacent Channel Rejection ACR (25 kHz offset single tone)
10 kHz	0	X	-116 dBm	20 dBc
9 kHz	1	139	-116 dBm	25 dBc
8 kHz	1	160	-115.5 dBm	30 dBc
7 kHz	1	185	-115 dBm	35 dBc

Table 8: Performances of the receiver for very narrow bandwidths and 4.8 kb/s

Table 9 below gives the sensitivity and the adjacent channel rejection for BR = 1.2 kbit/s and $\Delta f = 2$ kHz.

Bandwidth SSB	TParam_Low_BW	TParam_Code_BW(8:0)	Sensitivity RFS (BER=0.1%)	Adjacent Channel Rejection ACR (25 kHz offset single tone)
10 kHz	0	X	-117.5 dBm	18 dBc
9 kHz	1	139	-118 dBm	23 dBc
8 kHz	1	160	-119 dBm	28 dBc
7 kHz	1	185	-119.5 dBm	33 dBc

Table 9: Performances of the receiver for very narrow bandwidths and 1.2 kb/s

As expected, it can be seen from table 9 that this option also allows the sensitivity to be improved for very low bit rates and frequency deviations.

5.3 TRANSMITTER SECTION

The XE1205 is set to transmit mode when MCPParam_Select_mode is low by setting MCPParam_Chip_mode(1:0) to "10". If MCPParam_Select_mode is high the XE1205 is set to receive mode by setting pins SW(1:0) to "10".

The data directly modulates the LO, or an (optional) pulse shaping filter can be used resulting in an adjacent channel power down to -37dBm at 25kHz for an output power up to 10dBm.

In continuous mode the transmitted data is sent directly to the frequency synthesizer.

In buffered mode the data is first written into the sixteen byte FIFO via the SPI interface; data from the FIFO is used to modulate the frequency synthesizer.

5.3.1 Output Power

The output power of the power amplifier is programmable on four values with the register TXParam_Power (please refer to section 6.2.4 below), as shown in Table 10, where RFOP values are given in the Electrical Specifications section 4.2.2.

TXParam_POWER	Output power
0 0	RFOP1
0 1	RFOP2
1 0	RFOP3
1 1	RFOP4

Table 10: Output power settings

5.3.2 Transmitter in Continuous Mode

The transmitter works in continuous mode if the bit MCPParam_Buffered_mode is low. The transmit data should be applied to pin DATA if register bit Data_unidir is low or pin NSS_data if register bit Data_unidir is high. Figure 11 shows the transmitter chain in continuous mode:

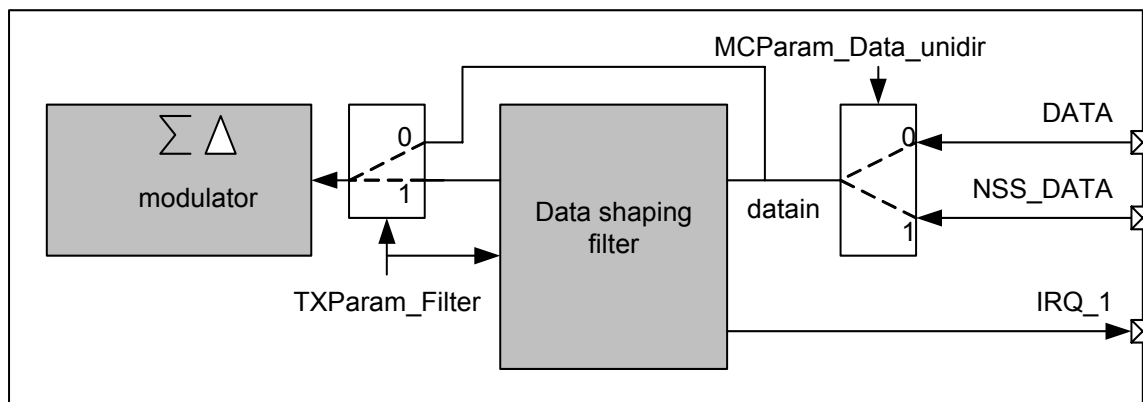


Figure 11: Transmitter data path in continuous mode

The pulse shaping function is enabled by setting TXParam_Filter to '1'. If the filtering option is selected, the DCLK signal is used as data clock in the transmission and this clock is generated at a frequency according to the selected bit rate. The DCLK signal is applied to the microcontroller via the pin IRQ_1, at the falling edge of each clock a new bit is supplied by the microcontroller. The data is sampled at the rising edge of DCLK and filtered.

Figure 12 shows an example of filtered data for a bit rate of 4.8kbit/s and a frequency deviation of 5 kHz:

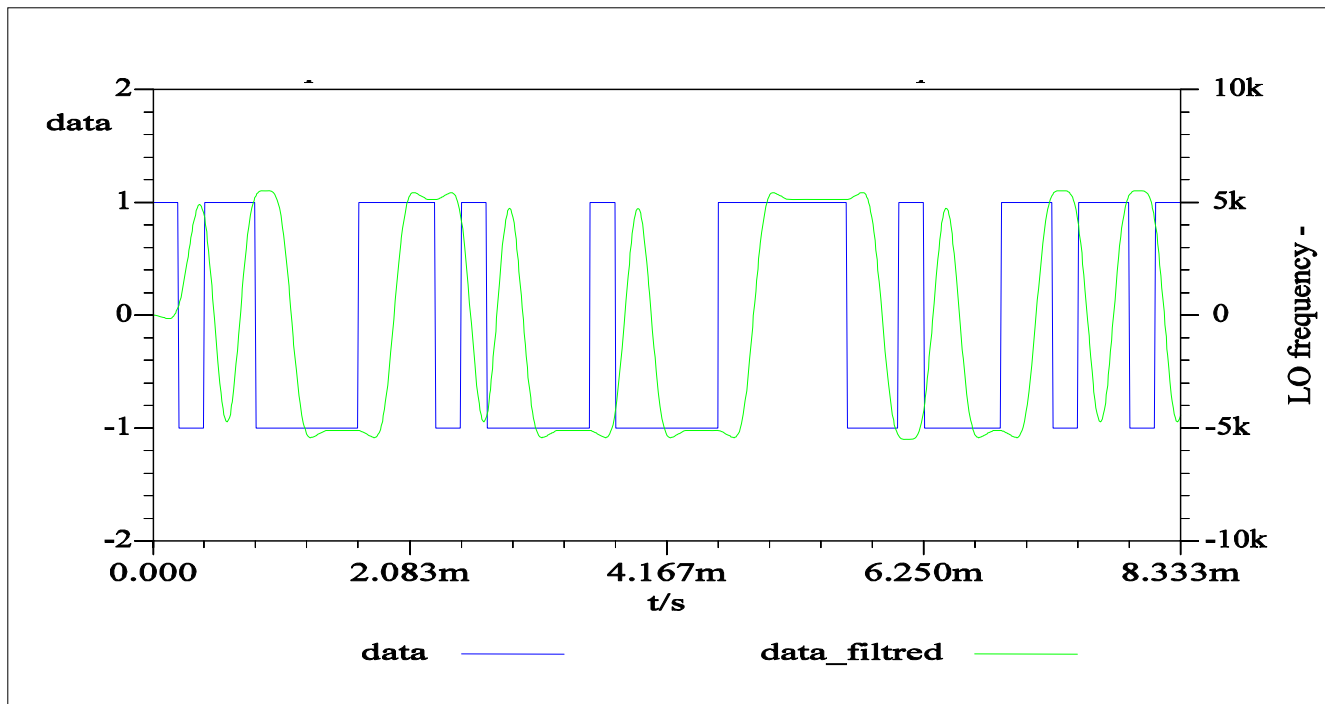


Figure 12: Pre-filtering of bit stream in transmit mode

The filtering option can be used for all bit rates specified in section 5.2.3.2 and for the following frequency deviations.

Freq_dev(8:0)	Frequency deviation (kHz)
000000101	2.5
000001010	5
000010100	10
000101000	20
001010000	40
010100000	80
101000000	160

Table 11: Available frequency deviations when using the filtering option

5.3.3 Transmitter in Buffered Mode

The transmitter works in buffered mode if bit `MCPParam_Buffered_mode` is high. Data to be transmitted is written to the 16-byte FIFO via the SPI interface. The data is loaded into a shift register which passes the data bit by bit to the data shaping filter or directly to the frequency synthesizer (as explained in the previous section). The transmitter chain is shown in Figure 13:

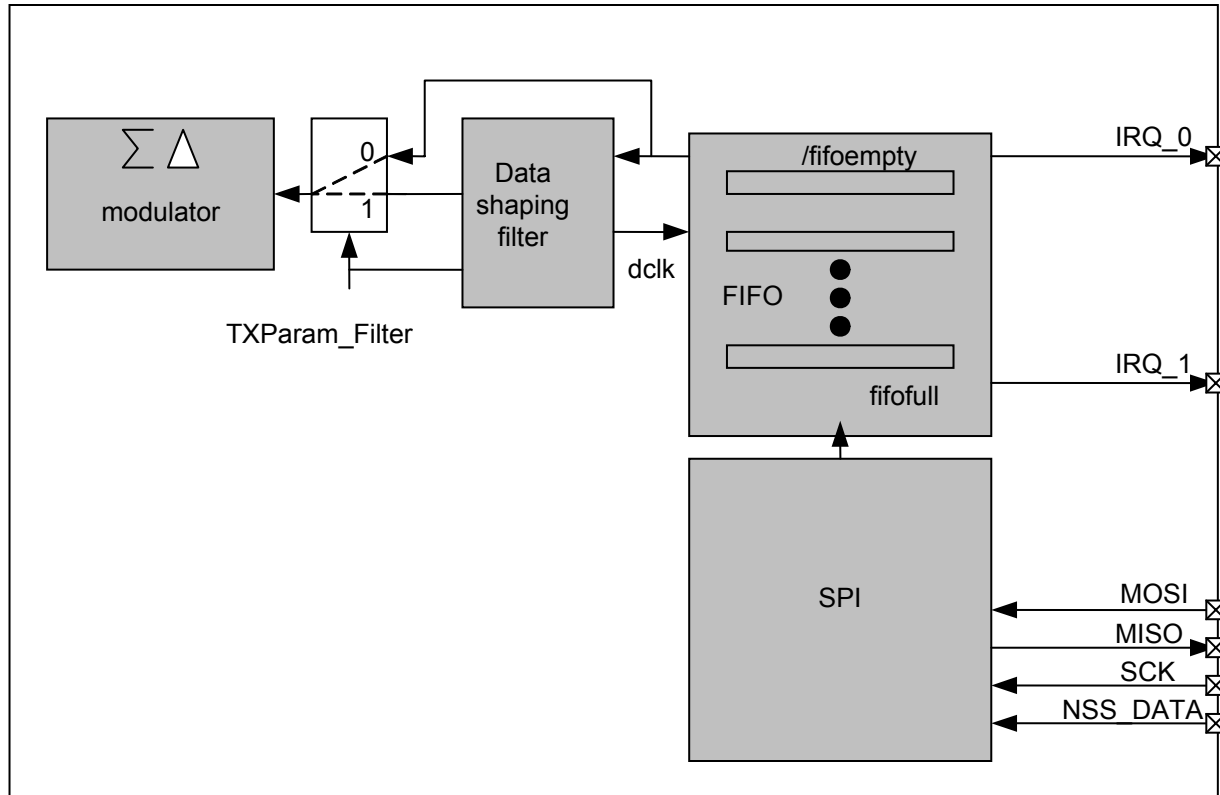


Figure 13: Transmit chain in buffered mode

FIFO operation in transmit mode is similar to receive mode; transmission either starts immediately after data is written into the FIFO or when the FIFO is full, determined by the `IRQParam_Start_full` bit setting.

If the transmit FIFO is full the interrupt signal `fifofull` is asserted on pin `IRQ_1`. If data is written into the FIFO while it is full, the flag `IRQParam_Fifooverrun` will be set to '1' and the previous FIFO contents will be overwritten.

The `IRQParam_Fifooverrun` flag is cleared by writing a '1' to it. At the same time this clears the contents of the FIFO. Once the last data in the FIFO is loaded into the shift register, the flag `/fifoempty` is set to high on pin `IRQ_0`. If new data is not written in the FIFO and the last bit of the shift register has been transferred to the frequency synthesizer, the bit `IRQParam_Tx_stopped` goes high and the data seen by the frequency synthesizer is the last bit sent. If the transmitter is switched off (e.g. entry into another mode), the transmission will stop immediately even if there is still unsent data in the shift register.

In transmit mode the two interrupt signals are `IRQ_0` and `IRQ_1`.

`IRQ_1` is mapped to `IRQParam_Fifofull` signal indicating that the transmission FIFO is full when `IRQParam_Tx_irq_1` is set to '0' and to `TX_stopped` when `IRQParam_Tx_irq_1` is set to '1'.

`IRQ_0` is mapped to the `/fifoempty` signal; this signal is used to indicate that the transmission FIFO is empty and must be refilled with data to continue data transmission.

5.4 FREQUENCY SYNTHESIZER

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver section as well as the continuous phase FSK (CPFSK) modulated signal for the transmitter section. The core of the synthesizer is implemented with a Sigma-Delta PLL architecture. The frequency is programmable with a minimum step-size of 500 Hz in the 433, 868 and 915 MHz frequency bands. This block includes a crystal oscillator which provides the frequency reference for the PLL. This reference frequency can also be used as a reference clock for the external microcontroller on the CLKOUT pin.

5.4.1 Clock Output for an External Processor

A reference clock can be generated for use by an external microcontroller. The OSCParam_Clkout configuration bit controls the CLKOUT pin. When set to high, CLKOUT is enabled, otherwise it is disabled. The output frequency at CLKOUT is defined by the value of the OSCParam_Clkout_freq(2:0) parameter. The output frequency at CLKOUT is the reference oscillator frequency divided by 2, 4, 8, 16 or 32. With a reference oscillator frequency of 39 MHz this provides a reference clock at 19.5 MHz, 9.75 MHz, 4.87 MHz, 2.44 MHz or 1.22 MHz, respectively.

This clock signal is disabled in Sleep Mode.

6 SERIAL INTERFACE DEFINITION AND PRINCIPLE OF OPERATION

6.1 SERIAL CONTROL INTERFACE

The XE1205 contains two SPI-compatible serial interfaces, one to send and read the chip configuration, the other to send and receive data in buffered mode. Both interfaces are configured in slave mode and share the same pins MISO (Master In Slave Out), MOSI (Master Out Slave In), SCK (Serial Clock). Two additional pins are required to select the SPI interface: NSS_config to change or read the transceiver configuration, and NSS_data to send or read data.

Figure 14 shows the connections between the transceiver and a microcontroller when buffered mode is used.

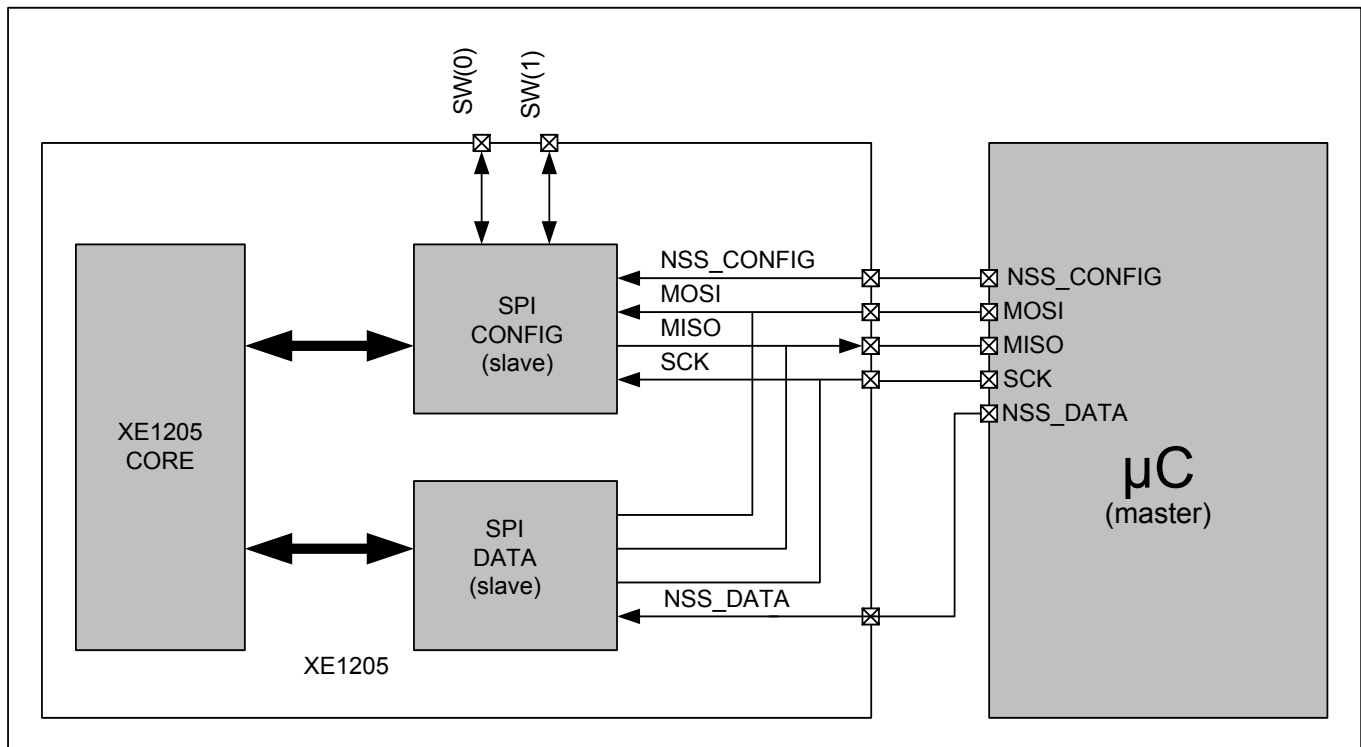


Figure 14: Connection between SPI DATA, SPI CONFIG and a micro-controller

By default, the serial control interface is used for configuration. It is also possible to change between the four modes (sleep, stand-by, receive, transmit) by using the two-bit signal SW(1:0). This option is enabled by setting the bit MCPParam_Select_mode to '1' in the configuration register.

A byte transmission can be seen as a rotate operation between the value stored in an 8 bit shift register of the master device (the microcontroller for instance) and the value stored in an 8 bit shift register of the selected slave device (the transceiver). The SCK line is used to synchronize both SPI interfaces. Data is transferred full-duplex from master to slave through the MOSI line and from slave to master through the MISO line. The most significant bit is always sent first. In both SPI interfaces the rising SCK edge is used to sample the received bit, and the falling SCK edge shifts the data inside the shift register.

The NSS_config or NSS_data signal is controlled by the master device and should remain low during the byte transmission. It is not necessary to toggle the NSS_config signal back to high and back to low between each transmitted byte. However It is necessary to toggle the NSS_data signal back to high and back to low between each transmitted byte. The transmission is synchronized by the NSS_config or NSS_data signal. While the NSS_config or NSS_data is high, the counters controlling transmission are reset. Reception starts with the first clock cycle after the falling edge of NSS_config or NSS_data; if either signal goes high during a byte transmission the counters are reset and the byte has to be retransmitted.

6.1.1 Chip Configuration via SPI_CONFIG Interface

The SPI_CONFIG interface is selected if NSS_config is low even if the circuit is in buffered mode and NSS_data is low (SPI_CONFIG has priority). To configure the transceiver two bytes are required; the first byte contains a start bit (equal to 0), R/W information ('1' for a read operation or '0' for a write operation), 5 bits for the address of the register and finally a stop bit (equal to '1'). The second byte contains the data to be sent in write mode or the new address to read from in read mode. Figure 15 shows the timing diagram for a typical write sequence:

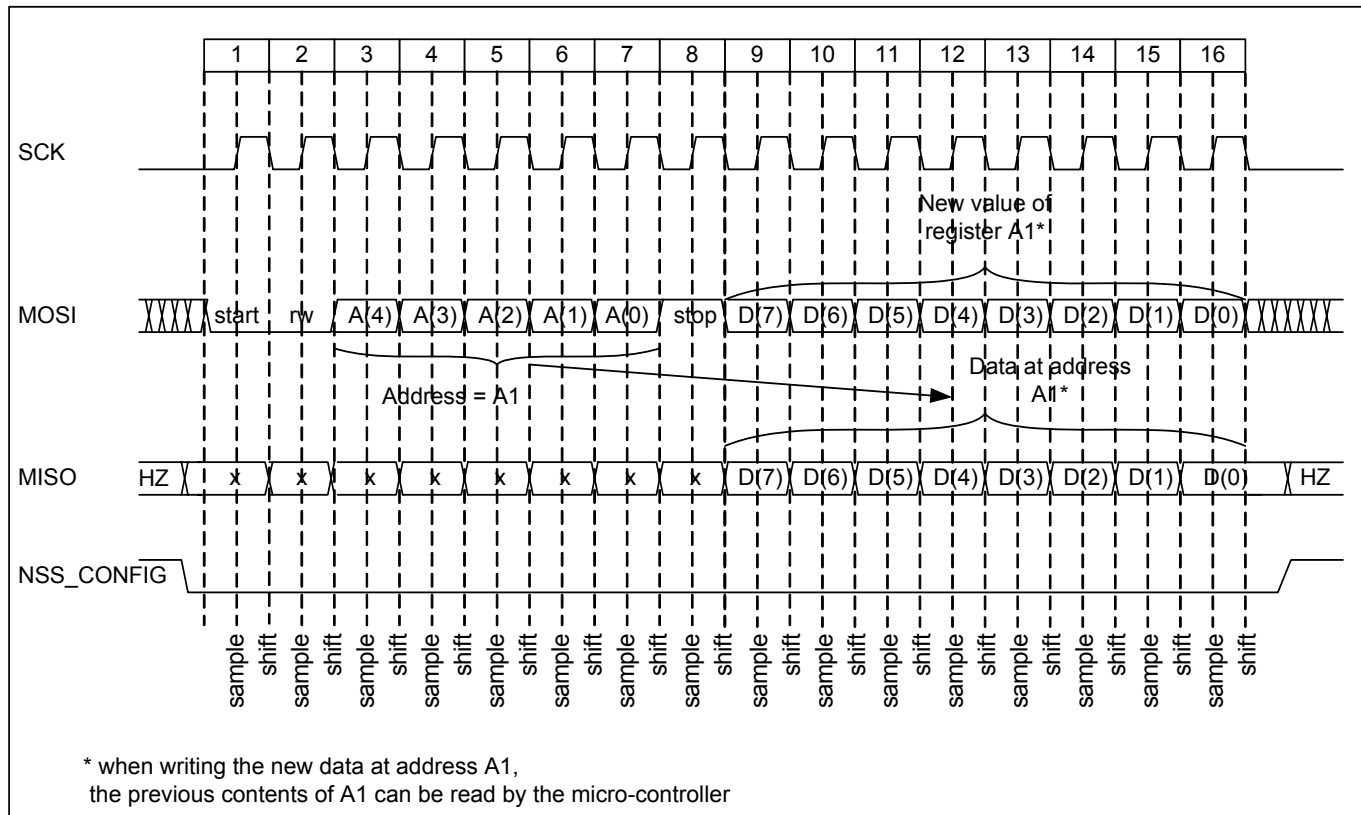


Figure 15: Write sequence when sending a new configuration to the XE1205 via the SPI_CONFIG

NSS_config must remain low during the transmission of the two bytes (address and data); if it goes high after the first byte, then the next byte will be considered as an address byte. When writing more than one register successively, NSS_config does not need to make a high to low transmission between two write sequences. The bytes are alternatively considered as an address byte followed by a data byte.

The read sequence via the SPI_CONFIG interface is similar to the write one except that the data byte contains all zeroes (if only one register is read) or the address of the next register to read (if more than one register is read). After sending the first address, the micro-controller will be able to send the next address to be read and to read the contents of the register at the previous address in the same time and so on.

Figure 16 shows the read sequence of a single register:

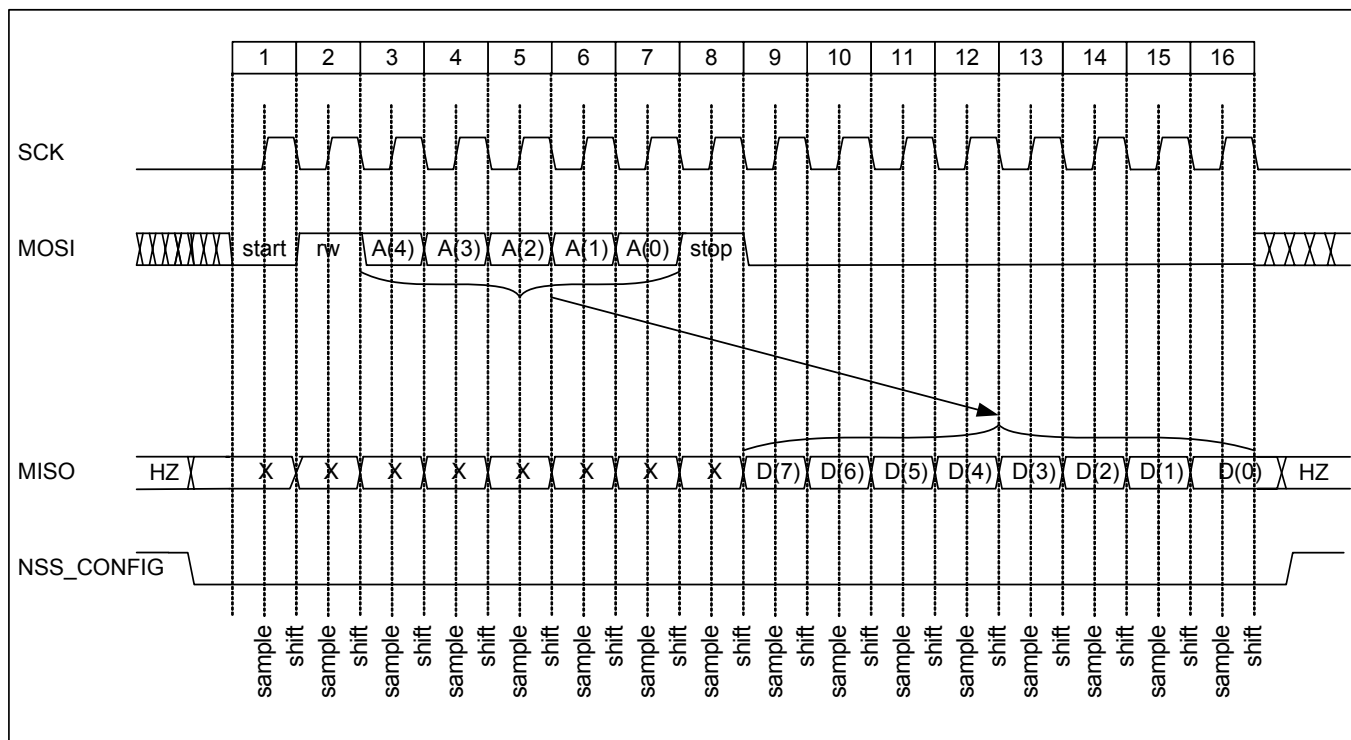


Figure 16: Read sequence of a single register via the SPI_CONFIG

Figure 17 shows the read sequence of two registers:

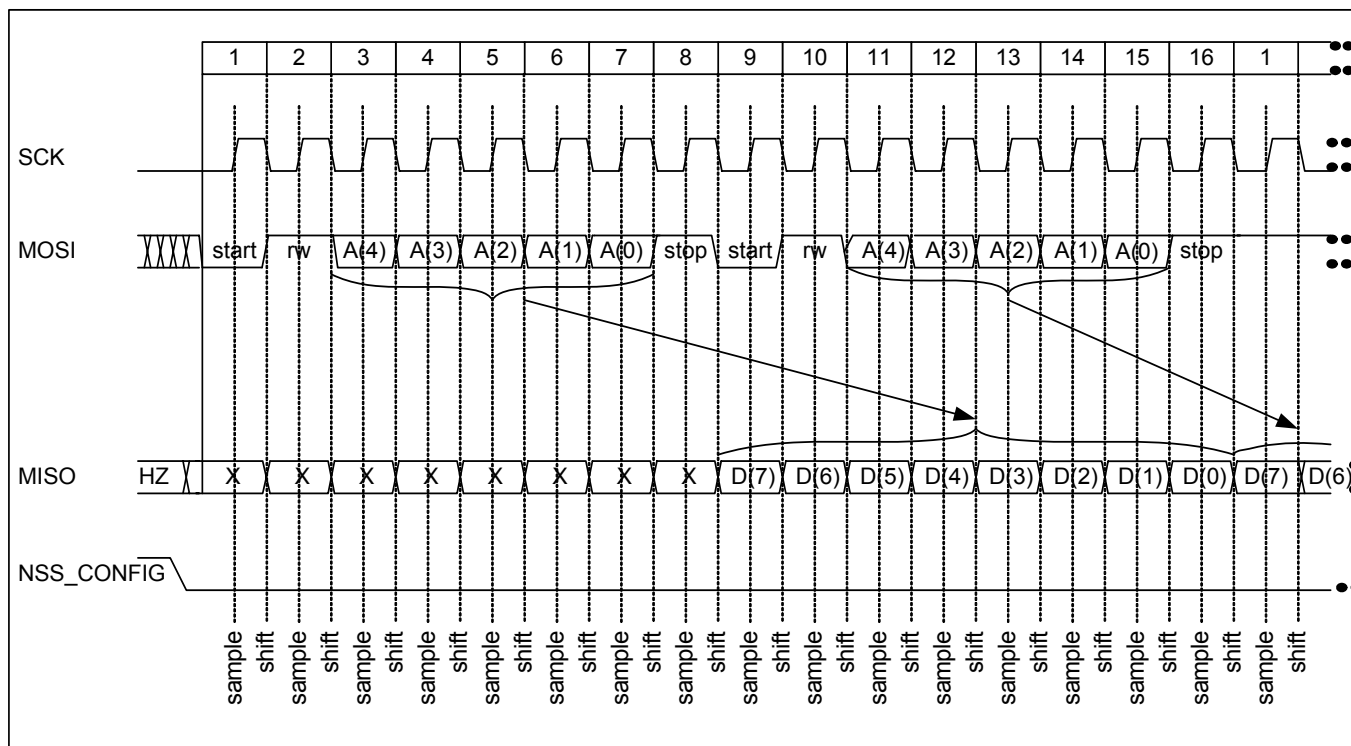


Figure 17: Read sequence of several registers via the SPI_CONFIG

6.1.2 Data Transmission and Reception via SPI_DATA Interface

When the transceiver is used in buffered mode, the data exchange with a micro-controller is via the SPI_DATA interface.

In transmit mode the 16 byte FIFO is filled whilst the interrupt signal IRQ_1 (TX_FIFOfull) is low.

In receive mode, the FIFO may be read if one of the following events occurs:

- at least one byte is present in the FIFO, i.e. a rising edge on IRQ_0 mapped to /fifoempty
- each time a byte is written to FIFO, i.e. a rising edge on IRQ_0 mapped to WRITE_BYTE
- 16 bytes have been written to the FIFO, i.e. a rising edge on IRQ_1 mapped to RX_FIFOfull

The transceiver should be in buffered mode (MCPParam_Buffered_mode = '1'). The SPI_DATA interface is then selected if NSS_data is low and NSS_config is high.

The operations with SPI_DATA interface are similar to those with SPI_CONFIG except that there is only a data byte (no address byte is required) and except that it is necessary to toggle the NSS_data signal back to high and back to low between each transmitted byte.

Figure 18 shows the write operation during transmit.

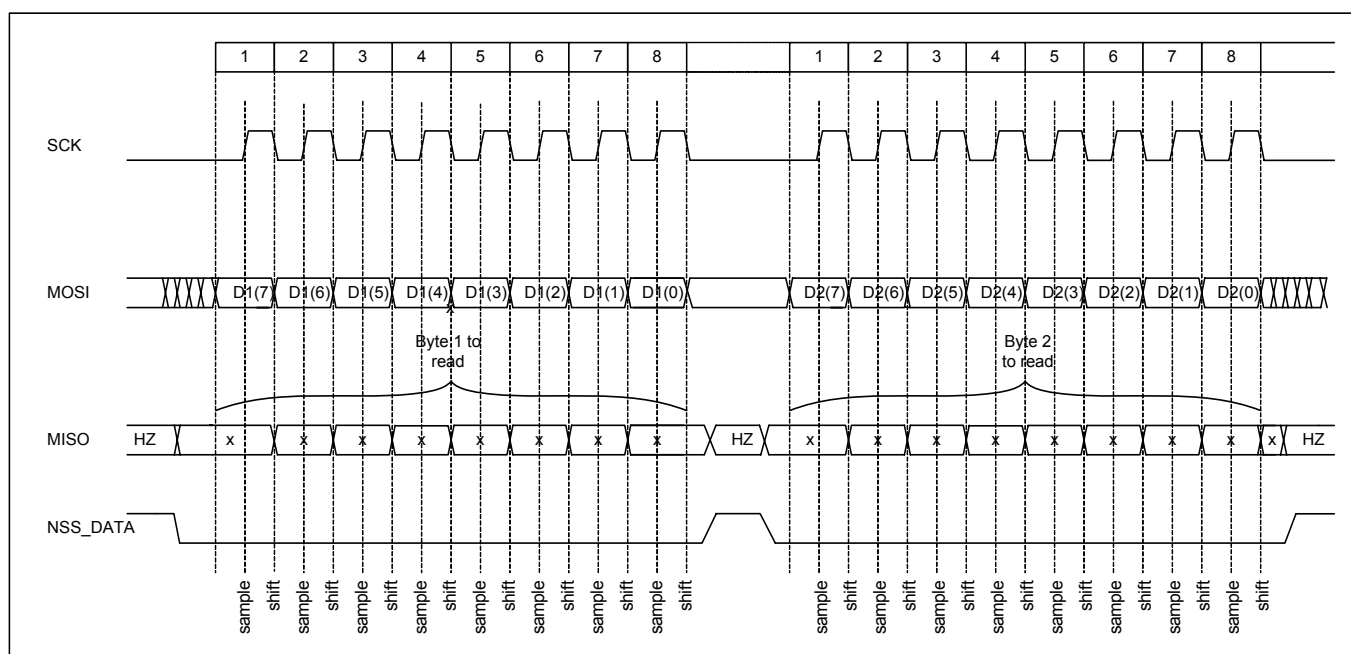


Figure 18: Writing 2 bytes in the FIFO when the XE1205 is in transmitter mode.

Figure 19 shows the read operation in receive mode.

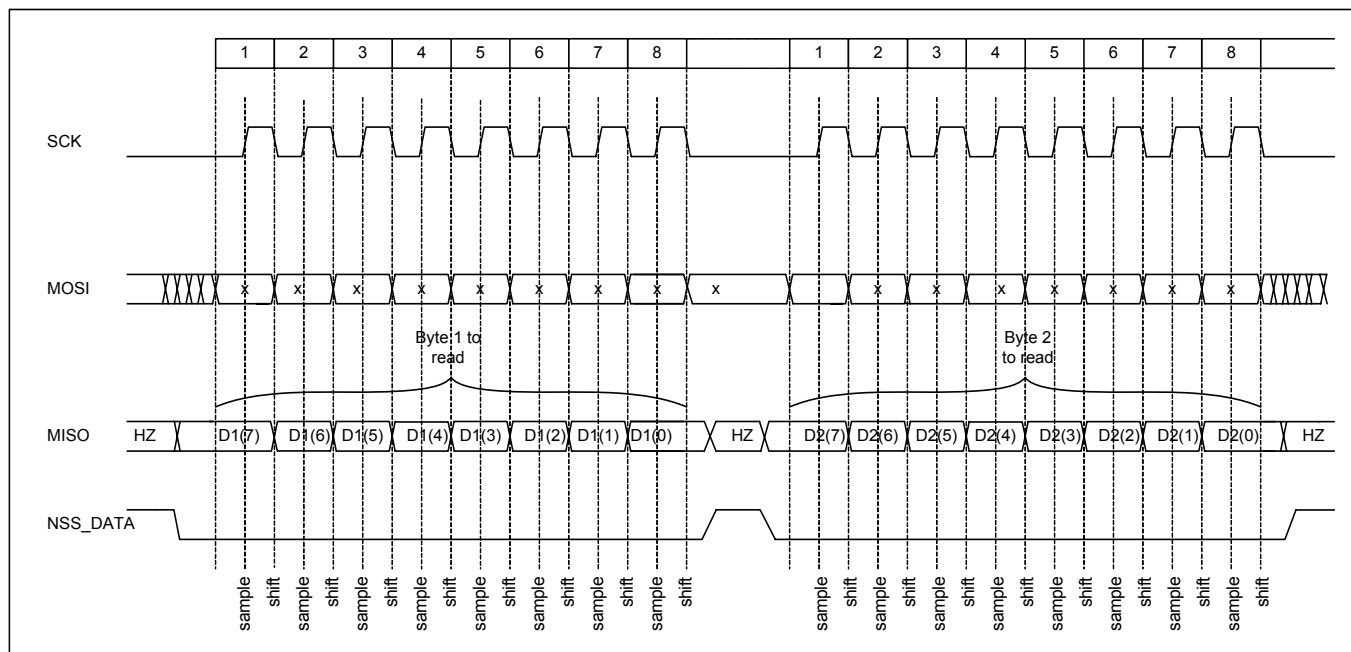


Figure 19: Reading 2 bytes in receive mode.

Note that it is necessary to toggle NSS_DATA signal back to high and then back to low between each transmitted byte.

6.2 CONFIGURATION AND STATUS REGISTERS

The XE1205 has several operating modes, configuration parameters and internal status registers. Some of the operating modes, the status information and the configuration parameters are stored in a series of internal Configuration and Status Registers that may be accessed by the microcontroller via the SPI_CONFIG interface.

The switching pins SW(1:0) allows switching between one of the four modes (sleep, stand-by, receive, transmit) when MCPParam_Select_mode is high. If MCPParam_Select_mode is low, the modes are defined by the register through the SPI_CONFIG interface and SW(1:0) may be used as an output to control, for example, an antenna switch.

6.2.1 Configuration Register: General Description

The description of the registers which are useful for the user is given in Table 12 below:

Name	Size	Address	Description
MCPParam	5 x 8	0-4	Main parameters common to transmit and receive modes
IRQParam	2 x 8	5-6	Interrupt registers
TXParam	1 x 8	7	Transmitter parameters
RXParam	9 x 8	8-16	Receiver parameters
OSCPParam	2 x 8	17-18	Oscillator parameters
TParam	12 x 8	19-30	Test and special settings

Table 12: configuration registers

All the bits that are referred to as “reserved” in this section should be set to “0” during write operations.

6.2.2 MCPParam Configuration Register (Main Configuration Parameters)

The detailed description of the MCPParam register is given in Table 13.

Name	Bits	Address	RW	Description
Chip_mode(1:0)	7-6	0	r/w	Transceiver mode: 00 -> sleep mode 01 -> receive mode 10 -> transmit mode 11 -> stand-by mode
Select_mode	5	0	r/w	Transceiver mode selection: 0 -> mode defined by MCPParam_chip_mode, SW(1:0) is an output sleep mode -> SW(1:0) = "00" receiver mode -> SW(1:0) = "01" transmitter mode -> SW(1:0) = "10" stand-by mode -> SW(1:0) = "00" 1 -> mode defined by SW(1:0) : SW(1:0) = 00 -> sleep mode SW(1:0) = 01 -> receive mode SW(1:0) = 10 -> transmit mode SW(1:0) = 11 -> stand-by mode
Buffered_mode	4	0	r/w	Enable buffered mode: 0 -> continuous mode 1 -> buffered mode
Data_unidir	3	0	r/w	Configure DATA pin 0 -> DATA is a bidirectional pin: input in transmit, output in receive mode 1 -> DATA is an output pin: output in receive mode, high-impedance in transmit mode
Band(1:0)	2-1	0	r/w	Frequency band: 01 -> 433 – 435 MHz 10 -> 868 – 870 MHz 11 -> 902 – 928 MHz
Freq_dev(8)	0	0	r/w	Frequency deviation MSB
Freq_dev(7:0)	7-0	1	r/w	Frequency deviation: $\Delta f = \text{int}(\text{Freq_dev}(8:0)) * \text{FSTEP}$ Where $\text{int}(x)$ = integer value of the binary representation of x Example 00000001 -> $\Delta f = \text{FSTEP}$ 11111111 -> $\Delta f = 511 * \text{STEP}$ all these frequency deviations are available if the data shaping filter is disabled (please refer to Table 11)
Knx	7	2	r/w	Konnex mode enable 0 -> default mode -> bit rate defined by MCPParam_Br(6:0) 1 -> Konnex mode -> bit rate = 32.7 kbit/s
Br(6:0)	6-0	2	r/w	Bit rate $\text{Br} = 152.34\text{e}3 / (\text{int}(\text{Br}) + 1)$ Where $\text{int}(x)$ = integer value of the binary representation of x. Example: 0000001 -> $\text{Br} = 76.1 \text{ kbit/s}$ 1111111 -> $\text{Br} = 1.19 \text{ kbit/s}$ Note: if Konnex mode is enabled, then bit rate = 32.7 kbit/s.

Name	Bits	Address	RW	Description
Freq_lo(15:8)	7-0	3	r/w	LO frequency in 2's complement representation configuration 1:
Freq_lo(7:0)	7-0	4	r/w	00...0 -> Flo = middle of the range 0X...X-> Flo = higher than the middle of the range 1X...X-> Flo = lower than the middle of the range Example: 00...001 -> Flo = middle of the range + FSTEP

Table 13: MCPParam configuration register

6.2.3 IRQParam Configuration Register (IRQ Parameters)

The detailed description of the IRQParam register is given in Table 14.

Name	Bits	Address	RW	Description
Rx_irq_0(1:0)	7-6	5	r/w	Select IRQ_0 sources in Rx mode: If Buffered_mode = 0 00 -> IRQ_0 mapped to Pattern signal 01 -> IRQ_0 mapped to RSSI_irq signal 10 -> IRQ_0 mapped to Pattern signal 11 -> IRQ_0 mapped to Pattern signal if Buffered_mode = 1 00 -> IRQ_0 set to '0' 01 -> IRQ_0 mapped to Write_byte signal 10 -> IRQ_0 mapped to /fifoempty signal 11 -> IRQ_0 mapped to Pattern signal
Rx_irq_1(1:0)	5-4	5	r/w	Select IRQ_1 sources in Rx mode If Buffered_mode = 0 00 -> IRQ_1 mapped to DCLK signal 01 -> IRQ_1 mapped to DCLK signal 10 -> IRQ_1 mapped to DCLK signal 11 -> IRQ_1 mapped to DCLK signal if Buffered_mode = 1 00 -> IRQ_1 set to '0' 01 -> IRQ_1 mapped to Fifofull signal 10 -> IRQ_1 mapped to RSSI_irq signal 11 -> IRQ_1 mapped to RSSI_irq signal
Tx_irq_1	3	5	r/w	Select IRQ_1 sources in Tx mode If Buffered_mode = 0 0 or 1 -> IRQ_1 is mapped to DCLK if Filter is high 0 or 1 -> IRQ_0 is set to low if Buffered_mode = 1 0 -> IRQ_1 is mapped to Fifofull signal 1 -> IRQ_1 is mapped to TX_stopped signal (IRQ_0 is mapped to /Fifoempty in Buffered mode)
Fifofull	2	5	r	FIFO full (IRQ source)
/fifoempty	1	5	r	FIFO empty (IRQ source)
Fifooverflow	0	5	r/w/c	FIFO overrun error : Write '1' clear FIFO
Start_fill	7	6	r/w	FIFO filling selection mode 0 -> The FIFO is filled if a pattern is detected 1 -> The FIFO is filled as long as Start_detect is high
Start_detect	6	6	r/w/c	Start of FIFO filling If start_fill = '0' goes high when a start sequence is detected writing a '1' clears the bit and wait for a new start sequence If start_fill = '1', 1 -> start to fill the FIFO, 0 -> stop to fill the FIFO.
Tx_stopped	5	6	r/w	Transmission stopped (IRQ source)
Start_full	4	6	r/w	0 -> Start transmission when the FIFO is full 1 -> start transmission when FIFL is not empty (/fifoempty = '1')

Name	Bits	Address	RW	Description
RSSI_int	3	6	r/w	Enable interrupt SIGNAL_DETECT when RSSI_thr is reached: 0 -> no interrupt generated 1 -> interrupt allowed
RSSI_signal_detect	2	6	r/w/c	Detection of a signal above RSSI_thr 0 -> signal power lower than the threshold defined by RSSI_thr. 1 -> signal power equal or greater than the threshold defined by RSSI_thr Writing '1' clear RSSI_signal_detect
RSSI_thr	1-0	6	r/w	RSSI threshold for interrupt 00 -> input power \geq VTHR1 01 -> input power \geq VTHR2 10 -> input power \geq VTHR3 11 -> input power \geq VTHR3

Table 14: IRQParam configuration register

6.2.4 TXParam Configuration Register (Transmitter Configuration Parameters)

The detailed description of the TXParam register is given in Table 15.

Name	Bits	Address	RW	Description
Power(1:0)	7-6	7	r/w	Transmitter output power: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
/Modul	5	7	r/w	Inhibition of the modulation in transmitter mode: 0 -> modulation 1 -> no modulation
Filter	4	7	r/w	Pre-filtering of the bit stream in transmitter mode: 0 -> no filtering 1 -> data shaping filter enabled all bit rates defined by Br are available frequency deviations given in Table 11 are available
RESERVED	3-2	7	r/w	RESERVED
Fix_bsync	1	7	r/w	0 -> bit sync in normal environment 1 -> bit sync in noisy environment
RESERVED	0	7	r/w	RESERVED

Table 15: TXParam configuration register

6.2.5 RXParam Configuration Register (Receiver Configuration Parameters)

The detailed description of the RXParam register is given in Table 16.

Name	Bits	Address	RW	Description
Disable_bitsync	7	8	r/w	Bit synchronizer on/off: 0 -> ON 1 -> OFF
BW(1:0)	6-5	8	r/w	Bandwidth of the base band filter: 00 -> 10 kHz 01 -> 20 kHz 10 -> 40 kHz 11 -> 200 kHz
Max_BW	4	8	r/w	Forces the bandwidth of the base band filter to its maximum value (about 400 kHz SSB) and disables calibration: 0 -> bandwidth defined by BW(1:0) 1 -> bandwidth forced to its maximal value

Name	Bits	Address	RW	Description
Reg_BW(1:0)	3-2	8	r/w	Calibration of the bandwidth of the base band filter: 00 -> calibration at start up 01 -> no calibration 10 -> calibration when the bandwidth of the base band filter changes 11 -> calibration is forced each time 11 is written
Init_filter(1:0)	1-0	8	r/w	Base band filter initialization: 00 -> default initialize at start up 01 -> RESERVED 10 -> initialize each time the bandwidth change 11 -> force re-initialization
RSSI	7	9	r/w	RSSI off/on: 0 -> off 1 -> on
RSSI_range	6	9	r/w	Range of the RSSI: 0 -> low range 1 -> high range
RSSI_out	5-4	9	r	00 -> input power \leq VTHR1 01 -> VTHR1 \leq input power \leq VTHR2 10 -> VTHR2 \leq input power \leq VTHR3 11 -> VTHR3 \leq input power
FEI	3	9	r/w	Frequency Error Indicator off/on: 0 -> off 1 -> on
RESERVED	2	9	r/w	RESERVED
RESERVED	1	9	r/w	RESERVED
RESERVED	0	9	r/w	RESERVED
RESERVED	7	10	r/w	RESERVED
IQAMP	6	10	r/w	IQ amplifier off/on: 0 -> off 1 -> on
Rmode	5	10	r/w	Linearity/sensitivity mode 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
Pattern	4	10	r/w	Pattern recognition off/on: 0 -> off 1 -> on
Psize(1:0)	3-2	10	r/w	Size of the reference Pattern: 00 -> 8 bits 01 -> 16 bits 10 -> 24 bits 11 -> 32 bits
Ptol(1:0)	1-0	10	r/w	Number of tolerated errors for the pattern recognition: 00 -> 0 error 01 -> 1 error 10 -> 2 errors 11 -> 3 errors
FEI_out(15:8)	7-0	11	r	MSB of FEI output
FEI_out(7:0)	7-0	12	r	LSB of FEI output

Table 16: RXParam configuration register

6.2.6 Pattern register

Name	Bits	Address	RW	Description
Reg_pattern(31:24)	7-0	13	r/w	1 st byte of the reference pattern
Reg_pattern(23:16)	7-0	14		2 nd byte of the reference pattern
Reg_pattern(15:8)	7-0	15		3 rd byte of the reference pattern
Reg_pattern(7:0)	7-0	16		4 th byte of the reference pattern

Table 17: Pattern register

This register holds the user supplied reference pattern of 8, 16, 24, or 32 bits (see the RXPParam_Psize(1:0) parameter). The first byte of this pattern is always stored in the byte at address 13. If used, the 2nd byte is stored at address 14, the 3rd byte at address 15 and finally the 4th byte at 16. The MSB bit of the reference pattern is always bit 7 of address 13.

Comparing the demodulated data, the first bit received of the last word is compared with bit 7 (the MSB) of byte address 13. The last bit received is compared with bit 0 (the LSB) in the Pattern register.

Table 18 provides an example of pattern recognition with a 32-bit pattern.

Byte Address 13 Bit 7 Bit 0	Byte Address 14 Bit 7 Bit 0	Byte Address 15 Bit 7 Bit 0	Byte Address 16 Bit 7 Bit 0
10010011	10101010	10010011	10101010
101 10010011	10101010	10010011	10101010
	previous bits from demodulator		last bit received

Table 18: Pattern recognition example (32 bits)

Table 19 provides an example of pattern recognition with an 8-bit pattern.

Byte Address 13 Bit 7 Bit 0	Byte Address 14 Bit 7 Bit 0	Byte Address 15 Bit 7 Bit 0	Byte Address 16 Bit 7 Bit 0
10010011	Xxxxxxxx	Xxxxxxxx	Xxxxxxxx
101 10010011			
previous bits from demodulator	last bit received		

Table 19: Pattern recognition example (8 bits)

6.2.7 OSCParam Configuration Register (Oscillator Parameters)

Name	Bits	Address	RW	Description
Osc	7	17	r/w	Sources of reference frequency 0 -> internal quartz oscillator 1 -> external signal applied on pin XTA
Clkout	6	17	r/w	Enable clkout 0 -> no signal provided on pin CLKOUT 1 -> Signal at reference frequency divided by 2, 4, 8, 16, 32 provided on CLKOUT (19.5 MHz down to 1.22 MHz)
Clkout_freq(2:0)	5-3	17	r/w	Frequency of signal provided on CLKOUT: 000 -> 1.22 MHz 001 -> 2.44 MHz 010 -> 4.87 MHz 011 -> 9.75 MHz others -> 19.5 MHz
RESERVED	2-0	17	r/w	RESERVED
Resxosc	7:5	18	r/w	Select the value of the resistor placed between TKA and TKB in order to use the transceiver with a crystal operating on its third overtone 0000 -> no resistor (3.8 MΩ) 0001 -> 1.48 kΩ 0010 -> 1.56 kΩ 0011 -> 1.66 kΩ 0100 -> 1.78 kΩ 0101 -> 1.91 kΩ 0110 -> 2.07 kΩ 0111 -> 2.26 kΩ 1000 -> 2.55 kΩ 1001 -> 2.81 kΩ 1010 -> 3.22 kΩ 1011 -> 3.79 kΩ 1100 -> 4.65 kΩ 1101 -> 6.04 kΩ 1110 -> 8.79 kΩ 1111 -> 16.55 kΩ
RESERVED	4-0	18	r/w	RESERVED

Table 20: OSCParam configuration register

6.2.8 TParam Configuration Register (Test And Special Settings)

Most of the parameters of this category are for test purposes. Some of them can be used to supersede settings that are described in previous sections to optimize special applications. These last parameters are described in the table below.

Name	Bits	Address	RW	Description
Add_BW	1	19	r/w	Change of RXParam_BW(1:0) decoding, allowing additional bandwidths for the base-band filter to be selected: Add_BW = 0 -> default values of RXParam_BW(1:0): RXParam_BW(1:0) = 00 => 10 kHz RXParam_BW(1:0) = 01 => 20 kHz RXParam_BW(1:0) = 10 => 40 kHz RXParam_BW(1:0) = 11 => 200 kHz Add_BW = 1 -> new bandwidth values: RXParam_BW(1:0) = 00 => 14.3 kHz RXParam_BW(1:0) = 01 => 28.5 kHz RXParam_BW(1:0) = 10 => 66.7 kHz RXParam_BW(1:0) = 11 => 100 kHz
Low_BW	2	19	r/w	Flag allowing selection of base-band filter bandwidths lower than 10 kHz: 0 -> default values given by RXParam_BW(1:0) and TParam_Add_BW 1 -> bandwidths defined by TParam_Code_BW(8:0)
Code_BW(8:0)	6-0 7-6	21 22	r/w	Low base-band filter bandwidths, when TParam_Low_BW = 1: Code_BW(8:0) = 139 => 9 kHz Code_BW(8:0) = 160 => 8 kHz Code_BW(8:0) = 185 => 7 kHz MSB Code_BW(8) = bit 6 of address 21
Add_HPF(2:0)	5-3	22	r/w	Cut-off frequency of the HPF stages allowing cancellation of the DC and low-frequency offsets in the baseband circuit: 0 0 0 -> 660 Hz (default value) 0 0 1 -> 1.48 kHz 0 1 0 -> 1.75 kHz 0 1 1 -> 1.96 kHz 1 0 0 -> 2.55 kHz 1 0 1 -> 3.34 kHz 1 1 0 -> 5.11 kHz 1 1 1 -> 10.2 kHz

Table 21: Useful special settings from TParam register

6.3 OPERATING MODES

The XE1205 has four main operating modes illustrated in Table 22 below. These modes are defined by register MCPParam_Chip_mode(1:0) when bit MCPParam_Select_mode is low and defined by SW(1:0) pins when MCPParam_Select_mode is high. The changes will be applied to the transceiver upon the rising edge of the NSS_CONFIG signal.

MCPParam_Select_mode	MCPParam_Chip_mode(1:0)	SW(1:0) mode	SW(1:0) value	Operating Mode	Enabled blocks of the transceiver
0	00	Output	00	Sleep	-
0	11	Output	00	Standby	Quartz oscillator
0	01	Output	01	Receive	Quartz oscillator, Frequency synthesizer, Receiver
0	10	Output	10	Transmit	Quartz oscillator, Frequency synthesizer, Transmitter
1	00	Input	00	Sleep	-
1	11	Input	11	Standby	Quartz oscillator
1	01	Input	01	Receive	Quartz oscillator, Frequency synthesizer, Receiver
1	10	Input	10	Transmit	Quartz oscillator, Frequency synthesizer, Transmitter

Table 22: Operating modes

6.3.1 XE1205 Switching Time Using SPI_CONFIG Interface

The transceiver is able to switch between modes by using the SPI_CONFIG interface.(MCPParam_Chip_mode(1:0)) or by using the pin SW(1:0). This section describes the switching sequence of the transceiver when register MCPParam_Select_mode is low i.e. the configuration is done via the SPI_CONFIG and SW(1:0) is an output.

The sequence from sleep mode to receive mode via stand-by mode is shown in Figure 20. TS_SRE is the receiver wake-up time when the oscillator is enabled, defined as the initialization time for the frequency synthesizer and the base band filter. The base band filter initialization and calibration processes occur when the transceiver switches from stand-by to receive.

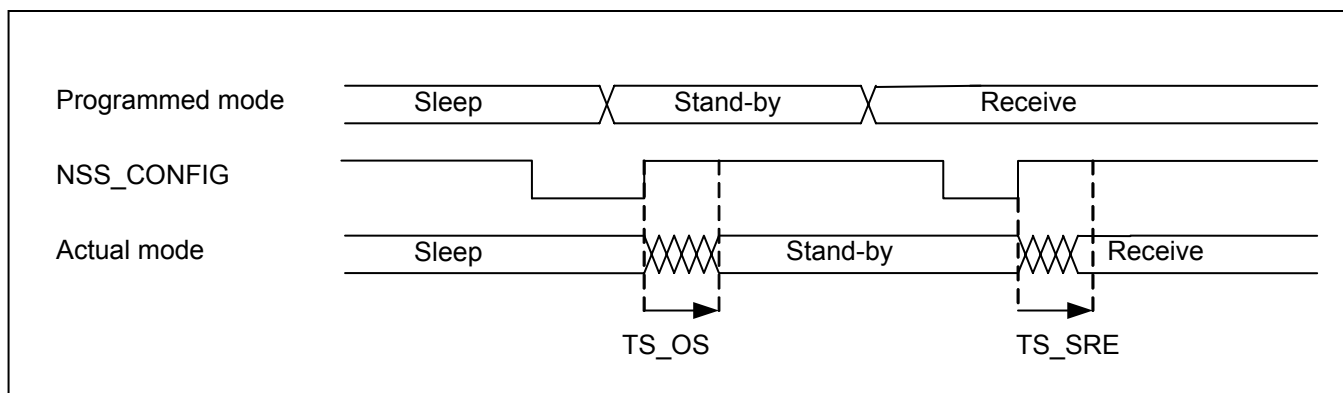


Figure 20: Sequence from sleep mode to receive mode via standby mode.

The sequence from sleep to transmit mode via stand-by mode is displayed in Figure 21. TS_STR is the initialization time of the frequency synthesizer and the power amplifier.

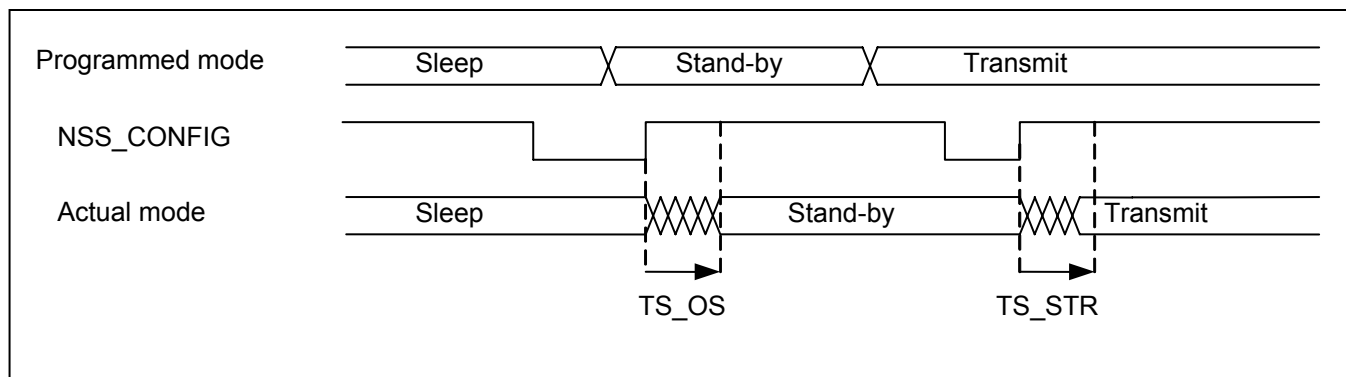


Figure 21. Sequence from sleep to transmit mode via stand-by mode.

The sequence from transmit to receive mode is shown in Figure 22. TS_RE is the initialization time of the receiver base band filter when the frequency synthesizer is enabled. The base band filter initialization and calibration processes occur when the transceiver switches from transmit to receive.

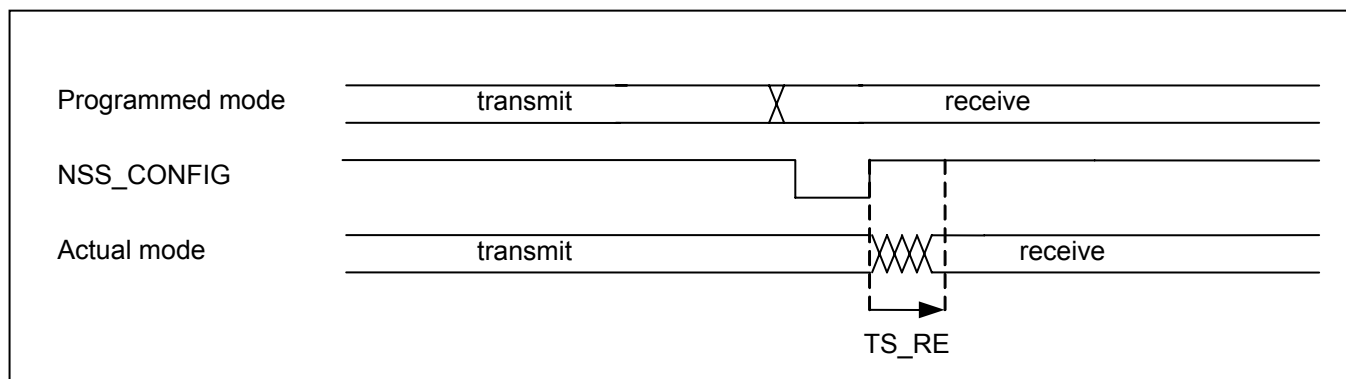


Figure 22: Sequence from transmit to receive mode.

Figure 23 represents the sequence from receive to transmit mode. TS_TR is the initialization time of the power amplifier if the frequency synthesizer is already enabled:

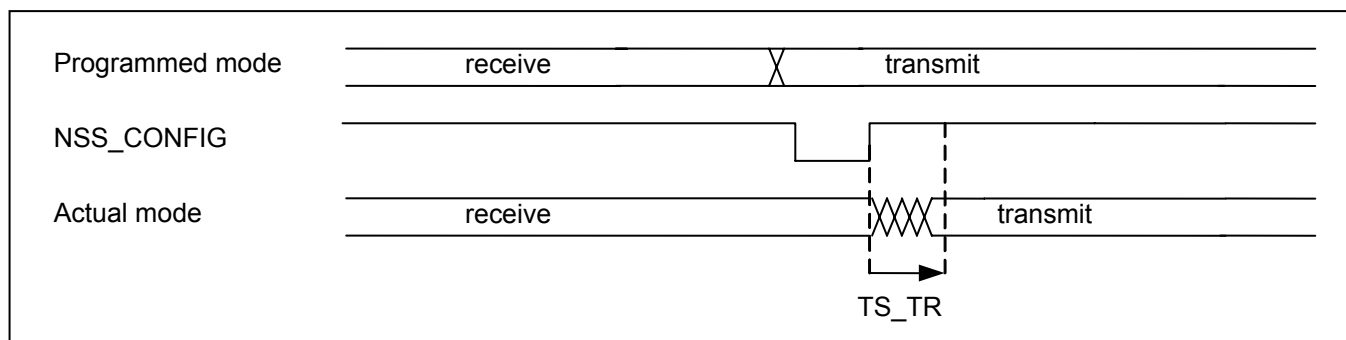


Figure 23: Sequence from receiver to transmitter mode

Figure 24 illustrates the switching time between two carrier frequencies in receive mode. TS_RFSW is defined as the switching time of the frequency synthesizer and the time needed by the base band filter to the steady-state when the boost process is used.

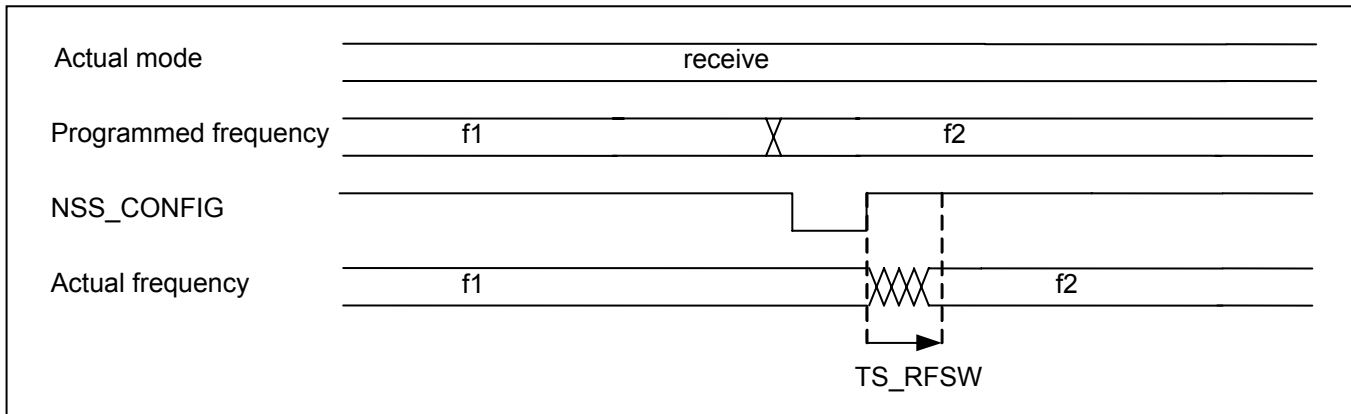


Figure 24. Switching between two carrier frequencies in receive mode.

Figure 25 shows the switching time between two carrier frequencies in transmit mode. TS_TFSW is defined as the switching time of the frequency synthesizer and the time required by the power amplifier to reaching the steady-state operating conditions.

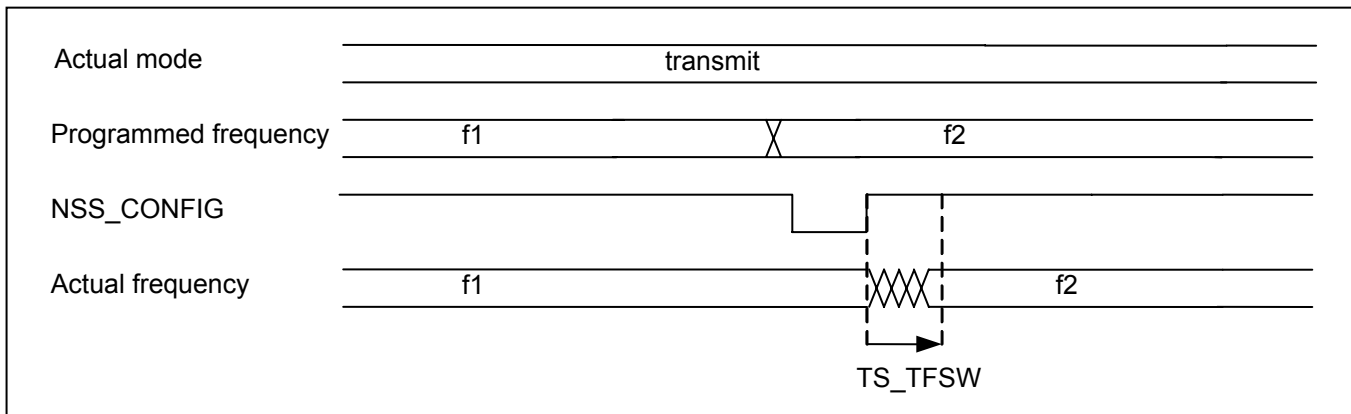


Figure 25. Switching between two carrier frequencies in transmit mode.

6.3.2 XE1205 Switching Time Using SW(1:0) Pins

If MCPParam_Select_mode is high then the transceiver mode is fixed by SW(1:0) pins and register MCPParam_Chip_mode can be used in read mode but has no effect on the transceiver mode.

6.4 SELECTION OF THE REFERENCE FREQUENCY

The reference clock used for the frequency synthesizer and the internal digital circuitry may be generated by an external 39 MHz quartz crystal or via an external oscillator. If an external oscillator is used, the register OSCParam_Osc has to be set high, and the 39 MHz external clock signal should be applied to the pin "XTA".

The transceiver can be used with a 39 MHz fundamental mode quartz crystal or with a 3rd overtone crystal. Third overtone operation requires an internal resistor to be connected in parallel with the crystal. This resistor can be connected by programming the register OSCParam_Resxosc(3:0). The required value depends on the crystal

specification. OSCParam_Resxosc(3:0) is set to "0000" by default, which selects a parallel resistor of 3.8 MΩ. This default value is used with a 39 MHz crystal enabled on its fundamental frequency.

In the case of overtone operation where the microcontroller uses the XE1205 as a clock source, the user should note that during the power up sequence of the XE1205, the oscillator may start and run at its fundamental frequency until the correct value of parallel resistor in the register OSCParam_Resxosc(3:0) is programmed. Before time-sensitive operations an oscillator settling period should be observed to ensure the desired oscillation frequency.

6.5 CLOCK OUTPUT INTERFACE

When OSCParam_Clkout is set high, a CLKOUT clock frequency is provided for a microcontroller or external circuitry. A user-programmable frequency divider ratio of 2, 4, 8, 16, 32 is selectable depending on OSCParam_Clkout_freq(2:0). The input frequency of this divider is the 39.0 MHz reference clock; the possible output frequencies are listed in Table 23:

OSC_Param_Clkout_freq(1:0)	CLKOUT frequency
000	1.22 MHz
001	2.44 MHz
010	4.87 MHz
011	9.75 MHz
others	19.5 MHz

Table 23: Frequency divider output

When the XE1205 is in sleep mode, CLKOUT is inactive even if bit OSCParam_Clkout remains high.

6.6 DEFAULT SETTINGS AT POWER-UP

The internally generated power on reset signal sets the MCPParam, RXParam, and TXParam registers to '0'. The only exception is the CLKOUT generation: though OSCParam_Clkout is set to low (i.e. disabled) the XE1205 provides a signal at 1.22 MHz on the pin CLKOUT.

The first rising edge on the NSS_CONFIG pin causes the registers to be updated and this will result in CLKOUT being disabled. For this reason the first programming sequence should be to enable CLKOUT by setting OSCParam_Clkout to high for applications using CLKOUT. It is recommended to initialize the XE1205 registers immediately after power-up.

6.7 PAD CONFIGURATION VERSUS CHIP MODES

The table below gives the pad configuration for the different chip modes and settings.

CHIP Mode \ PAD	Sleep	Standby	Receive	Transmit	Comment
SW0	OUTPUT when Select_mode = '0' else High Impedance	OUTPUT when Select_mode = '0' else High Impedance	OUTPUT when Select_mode = '0' else High Impedance	OUTPUT when Select_mode = '0' else High Impedance	If Select_mode = '1', SW0 and SW1 defined the chip mode
SW1	OUTPUT when Select mode = '1' else High Impedance	OUTPUT when Select mode = '1' else High Impedance	OUTPUT when Select mode = '1' else High Impedance	OUTPUT when Select mode = '1' else High Impedance	If Select_mode = '1', SW0 and SW1 defined the chip mode
NSS_CONFIG	INPUT	INPUT	INPUT	INPUT	NSS_CONFIG has the priority over NSS_DATA
NSS_DATA	INPUT	INPUT	INPUT	INPUT	NSS_DATA is used as data modulation input if Data_unidir is high
IRQ_0	High impedance	High impedance	OUTPUT	OUTPUT	

CHIP Mode	Sleep	Standby	Receive	Transmit	Comment
PAD					
IRQ_1	High impedance	High impedance	OUTPUT	OUTPUT	
DATA	High impedance	High impedance	OUTPUT	High impedance	
CLKOUT	OUTPUT	OUTPUT	OUTPUT	OUTPUT	
MISO	OUTPUT if NSS_CONFIG='0' or NSS_DATA = '0'	OUTPUT if NSS_CONFIG='0' or NSS_DATA = '0'	OUTPUT if NSS_CONFIG='0' or NSS_DATA = '0'	OUTPUT if NSS_CONFIG='0' or NSS_DATA = '0'	
MOSI	INPUT	INPUT	INPUT	INPUT	
SCK	INPUT	INPUT	INPUT	INPUT	

Table 24. Pad configuration vs chip modes

7 APPLICATION INFORMATION

This section provides details of the recommended component values for the frequency dependant blocks of the XE1205. Note that these values are dependent upon circuit layout and PCB structure, and that decoupling components have been omitted for clarity.

7.1 MATCHING NETWORK OF THE RECEIVER

The schematic of the matching network at the input of the receiver is given below (for a source impedance of 50Ω).

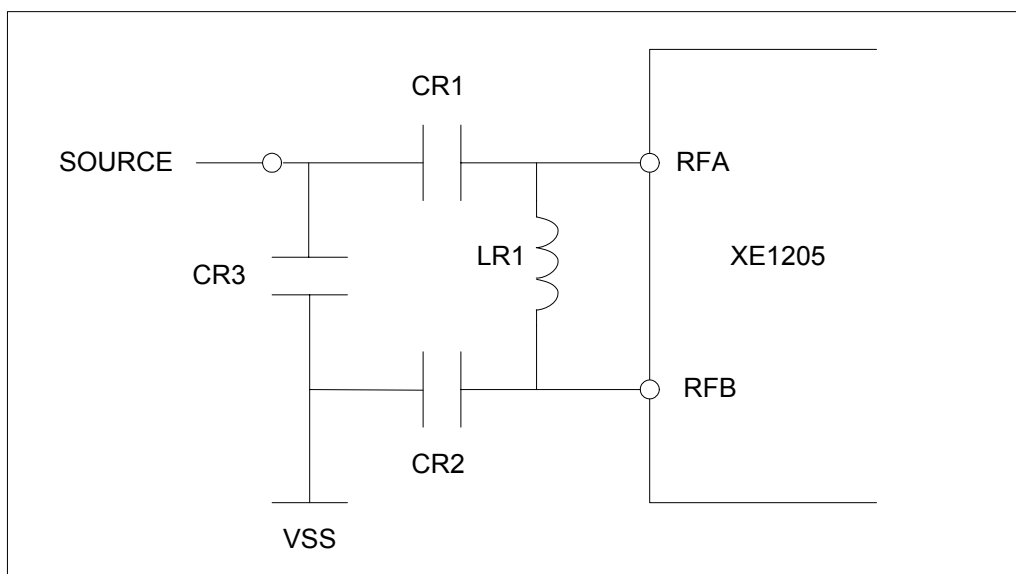


Figure 26 Matching network at the input of the receiver.

The typical component values of the matching circuit are shown in Table 25 below.

Name	Typical Value for 434 MHz	Typical Value for 869 MHz	Typical Value for 915 MHz	Tolerance
CR1	1.5pF	1.2pF	1.2pF	$\pm 5\%$
CR2	1.5pF	1.5pF	1.2pF	$\pm 5\%$
CR3	NC	NC	NC	$\pm 5\%$
LR1	100nH	27nH	27nH	$\pm 5\%$

Table 25: Matching network values

7.2 MATCHING NETWORK OF THE TRANSMITTER

The optimum load impedances for 15 dBm output power at the three main frequencies are given in Table 26.

	434 MHz	869 MHz	915 MHz
PA optimum load	$89 - j19$	$80 + j17$	$84 + j11$

Table 26: Optimum load impedances for 15dBm output power

The Smith charts in Figure 27 and Figure 28 below show contours of output power versus load impedance when the highest output level is selected (15 dBm mode).

869 MHz 15 dBm

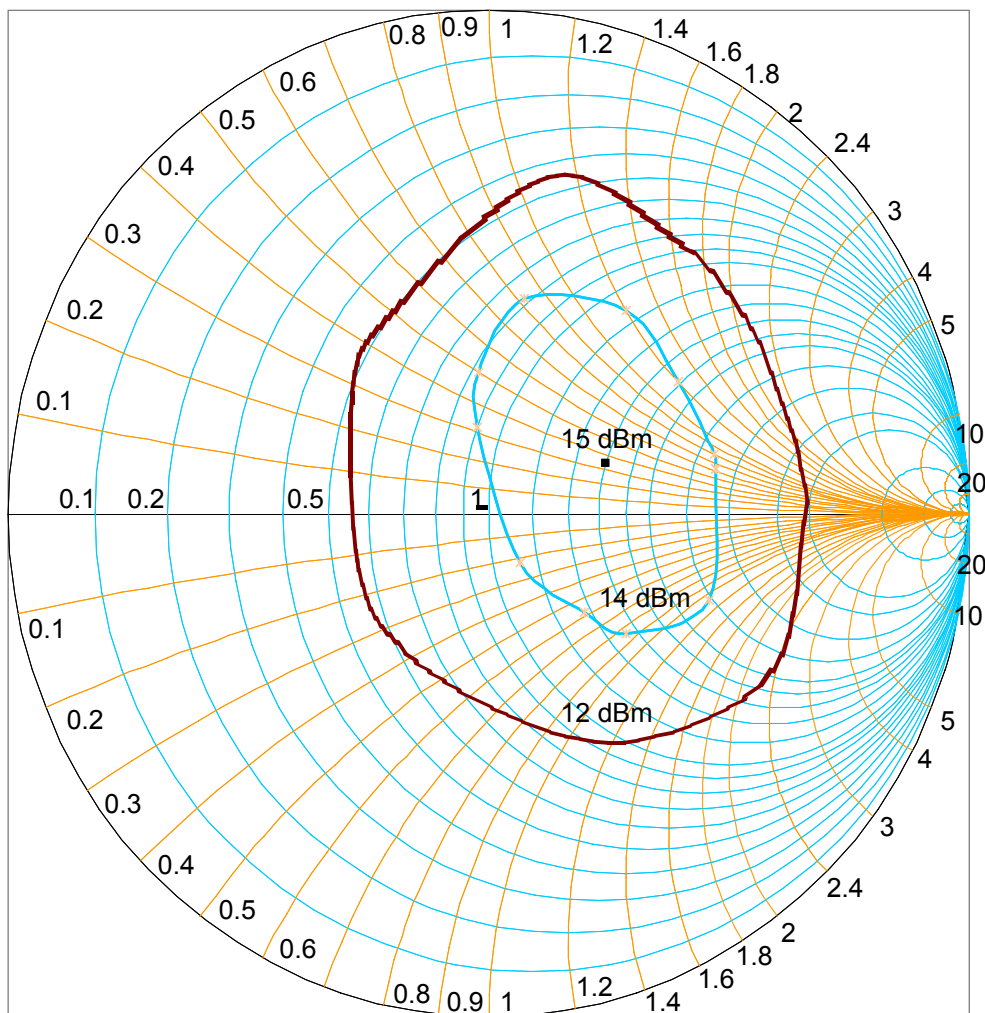


Figure 27: Output power vs. load impedance at 869 MHz.

915 MHz 15 dBm

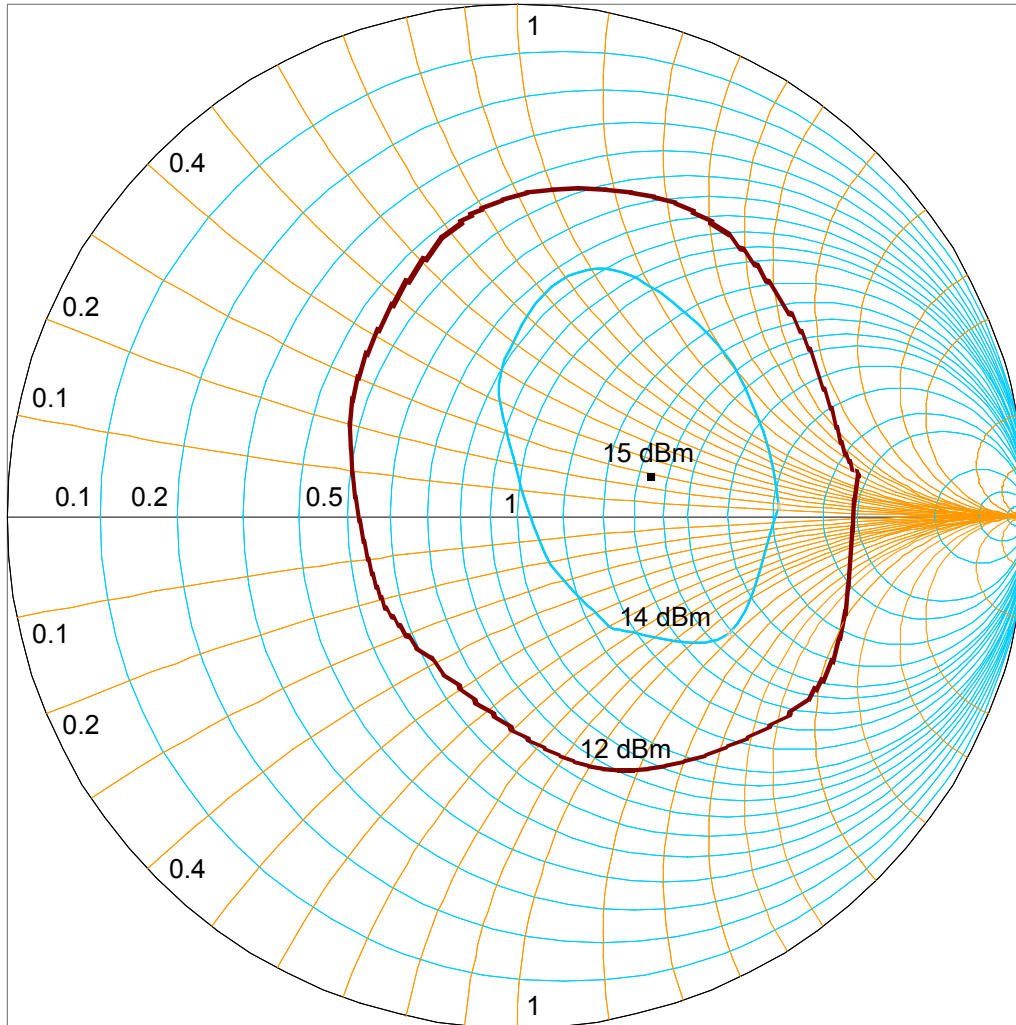


Figure 28: Output power vs. load impedance at 915 MHz.

The schematic of the recommended matching network at the output of the transmitter is given in Figure 29 below. The two Π -sections are used to provide harmonic filtering to satisfy FCC and ETSI regulations.

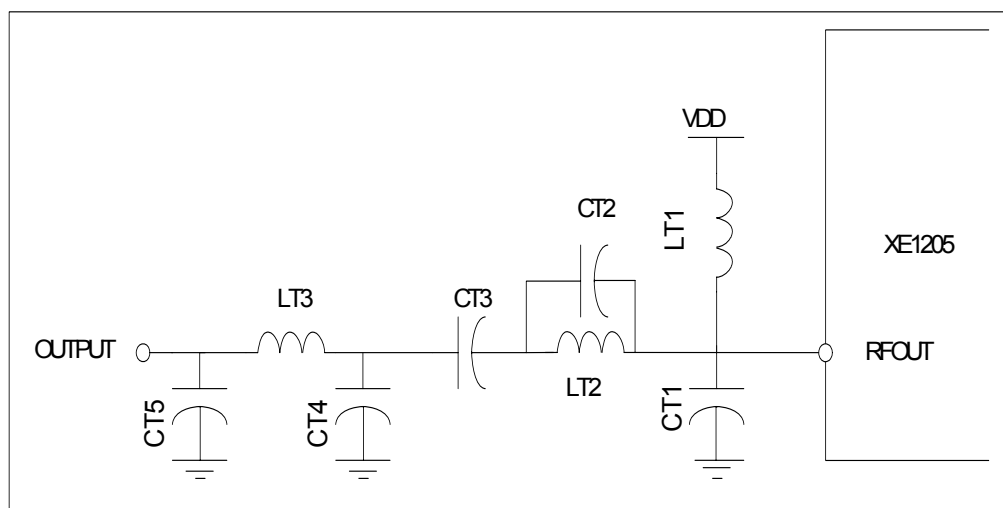


Figure 29 Matching network at the output of the transmitter.

The typical component values of the matching circuit are shown in Table 27 below.

Name	Typical Value for 434 MHz	Typical Value for 869 MHz	Typical Value for 915 MHz	Tolerance
CT1	6.8 pF	1.5 pF	1.8 pF	$\pm 5\%$
CT2	1.0 pF	0.56 pF	NC	$\pm 5\%$
CT3	22 pF	15 pF	33 pF	$\pm 5\%$
CT4	6.8 pF	3.3 pF	3.3 pF	$\pm 5\%$
CT5	4.7 pF	2.2 pF	2.2 pF	$\pm 5\%$
LT1	33 nH	39 nH	47 nH	$\pm 5\%$
LT2	22 nH	10 nH	10 nH	$\pm 5\%$
LT3	22 nH	8.2 nH	8.2 nH	$\pm 5\%$

Table 27: Matching circuit component values

7.3 VCO TANK

The VCO tank circuit should be implemented with an inductor and capacitor in parallel. Typical component values are shown in Table 28.

Name	434 MHz	869 MHz	915 MHz	Tolerance
CV1	1.0 pF	NC	NC	$\pm 5\%$
LV1	33 nH	6.8 nH	5.6 nH	$\pm 2\%$

Table 28: VCO tank component values

7.4 LOOP FILTER OF THE FREQUENCY SYNTHESIZER

The loop filter of the frequency synthesizer is shown in Figure 30 below.

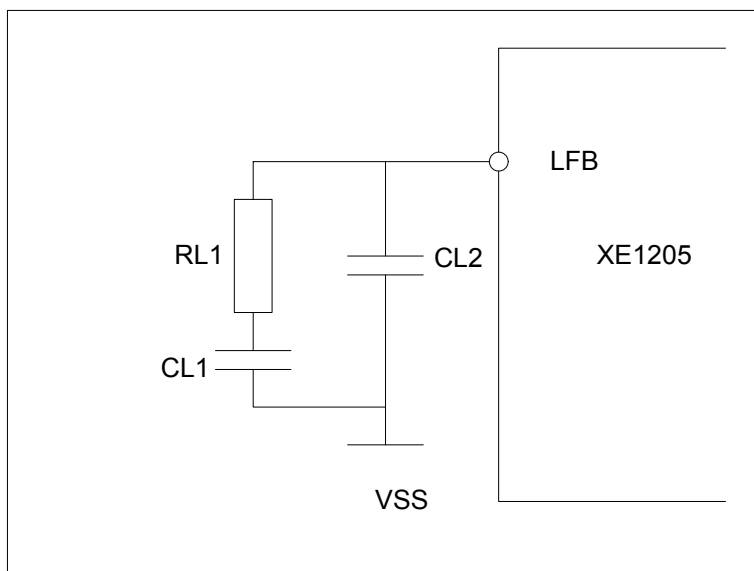


Figure 30: Frequency synthesizer loop filter

Typical recommended component values for the frequency synthesizer loop filter are provided in Table 29 below:

Name	434 MHz	869 MHz	915 MHz	Tolerance
CL1	22 nF	12 nF	10 nF	± 5%
CL2	1 nF	1 nF	1 nF	± 5%
RL1	560Ω	560Ω	680Ω	± 5%

Table 29: Typical frequency synthesizer component values

7.5 REFERENCE CRYSTAL FOR THE FREQUENCY SYNTHESIZER

For narrow band applications, where users select the lowest frequency deviation and the narrowest baseband filter, the crystal for reference oscillator of the frequency synthesizer should have the following typical characteristics:

Name	Description	Min. value	Typ. value	Max. value
Fs	Nominal frequency	-	39.0 MHz (fundamental)	-
CL	Load capacitance for fs (on-chip)	-	8 pF	-
Rm	Motional resistance	-	-	40Ω
Cm	Motional capacitance	-	-	30 fF
C0	Shunt capacitance	-	-	7 pF
$\Delta f_s(0)$	Calibration tolerance at 25 °C	-	-	10 ppm
$\Delta f_s(\Delta T)$	Stability over temperature range (-40 °C to 85 °C)	-	-	10 ppm
$\Delta f_s(\Delta t)$	Aging tolerance in first 5 years	-	-	5 ppm

Table 30: Crystal characteristics

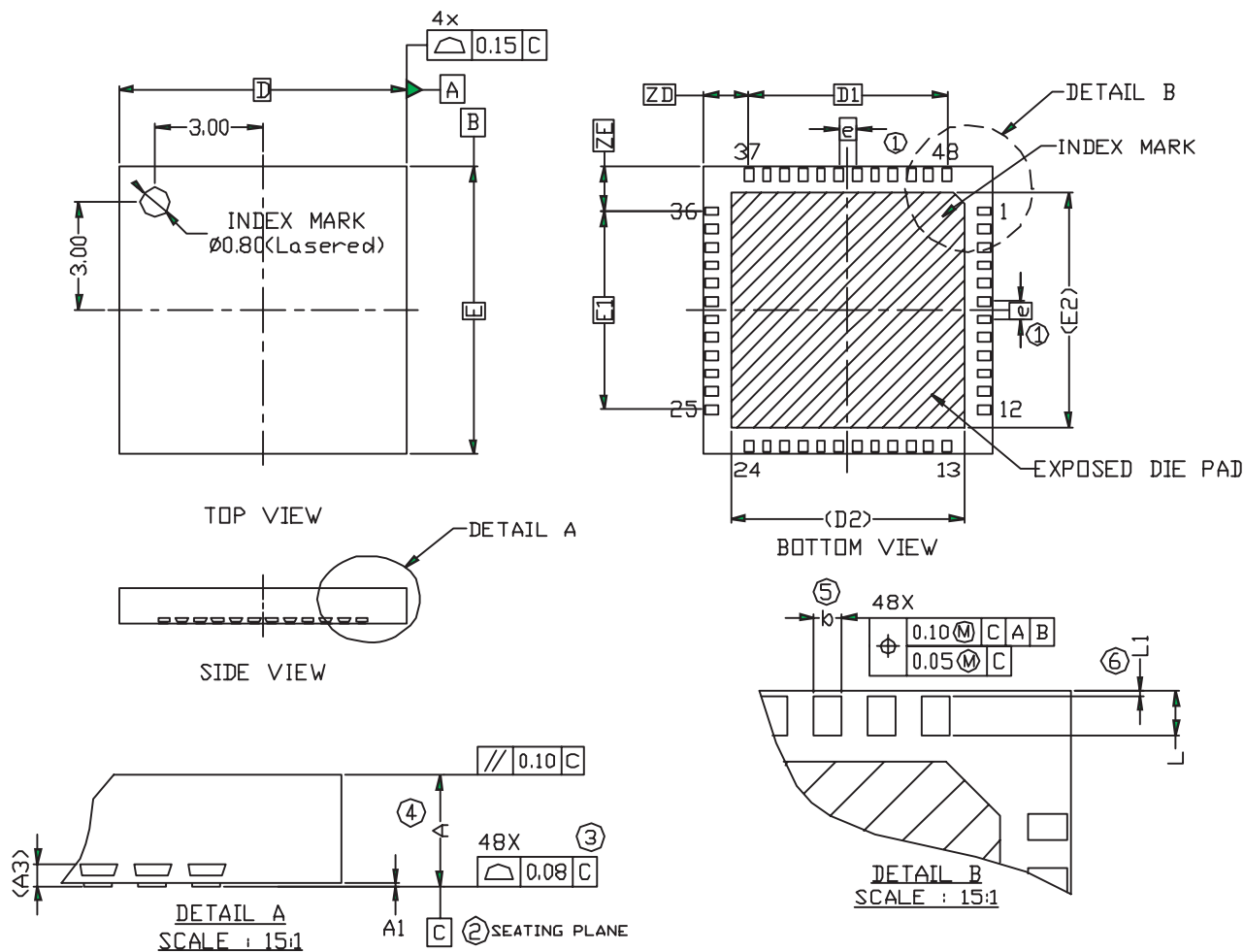
The electrical specifications given in section 4.2.2 are valid for a crystal having the specifications given in Table 30. For wide band applications requiring less frequency stability, the values for $\Delta f_s(0)$, $\Delta f_s(\Delta T)$, and/or $\Delta f_s(\Delta t)$ can be relaxed. In this case $\text{offset} + \text{BW}_{\text{ssb}}$ should be lower than $\text{BW}_{\text{filter}}$, where offset is the offset (error) on the carrier frequency (the sum of $\Delta f_s(0)$, $\Delta f_s(\Delta T)$, and/or $\Delta f_s(\Delta t)$), BW_{ssb} is the single side-band bandwidth of the signal, and $\text{BW}_{\text{filter}}$ is the single side-band bandwidth of the base-band filter.

The overtone crystal usage can result in higher oscillator start-up time than fundamental mode. The overtone crystal should be designed for $C_{\text{load}} = 8$ to 10 pF and has parameters of $R_m < 60\Omega$, $C_0 < 7$ pF.

8 PACKAGING INFORMATION

XE1205 comes in a 48-lead VQFN 8X8 package as shown in Figure 31 below.

Figure 31: Package dimensions



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	0.80	0.90
A1	0	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	8.00 BSC		
D1	5.50 BSC		
E	8.00 BSC		
E1	5.50 BSC		
e	0.50 BSC		
L1	0.03	—	0.15
L	0.30	0.40	0.50
D2	6.50 ~ 6.80 Ref		
E2	6.50 ~ 6.80 Ref		
ZD	1.25 BSC		
ZE	1.25 BSC		

NOTES:

- ① 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
- ② DATUM 'C' IS THE MOUNTING SURFACE, WITH WHICH THE PACKAGE IS IN CONTACT.
- ③ SPECIFIES THE VERTICAL SHIFT OF THE FLAT PART OF EACH TERMINAL FROM THE MOUNTING SURFACE.
- ④ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
- ⑤ DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION 'b' SHOULD NOT BE MEASURED IN THE RADIUS AREA.
- ⑥ DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT. L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.3mm.
- 7 PACKAGE DIMENSIONS CONFORM TO JEDEC MO-220 Rev.H, VARIATIONS VLLD

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