Passive Components ▬▬▬

Specifying a quartz crystal for a VCXO

A popular application for the voltage-controlled crystal oscillator is the forming of a phase-locked loop. Designing the VCXO for this application requires a 'pullable' quartz crystal.

By Ramon M. Cerda

A voltage-controlled crystal oscillator's (VCXO) output frequency changes in direct proportion to the application of an input control voltage. One of the most common uses for a VCXO is to form a phase-locked loop (PLL) to synchronize, translate (up or down), and/or de-jitter an input reference frequency. The design of a VCXO requires specifying a *pullable crystal*.

Crystal parameters

The most popular use of a VCXO is in a PLL application, as shown in Figure 1. The electrical equivalent circuit of the quartz crystal used in the VCXO is shown in Figure 2. *C1*, *L1* and *R1* are called the motional parameters of the crystal, and *C0* is the shunt capacitance. *C0* is real—it can actually be measured with a simple capacitance meter. The motional arm parameters, on the other hand, are equivalents and not simple to measure. How much the frequency of the crystal is pulled or deviated will depend on the ratio of *C0/C1*.

The impedance equation of Figure 2 is:

$$Z(jw) = \frac{(1/jwC1 + jwL1 + R1)(1/jwC0)}{(1/jwC1 + jwL1 + R1) + (1/jwC0)} \quad (1)$$

Equation 1 is complex, and we are interested in the imaginary part only, which is called the crystal's reactance curve and is depicted in Figure 3.

In Figure 3, the point marked as *fs* is where the motional capacitance *C1* resonates and cancels the motional inductance *L1*. A crystal calibrated to the desired frequency at *fs* is called a series crystal. A crystal calibrated to work in the area of parallel resonance is called a parallel crystal. It's important to note here that there's no difference between a series and a parallel crystal, only where it is calibrated by the manufacturer.

A VCXO circuit will effectively place a load capacitance (*CL*) in series with the terminals of the crystal. As the load capacitance is varied, the crystal will respond by changing its frequency on the area of parallel resonance. This is tricky and is misstated in many papers. The capacitive load is always placed effectively in series with the crystal and never in parallel. In other words, a so-called parallel crystal does not mean you place a capacitor in parallel with the crystal, but in series.

Load capacitance is the capacitance needed to be placed in series with a parallel crystal to bring the frequency within the calibration tolerance.

As mentioned above, as the load capacitance *CL* is varied, the frequency of the crystal changes. In fact, it changes as follows:

$$\frac{\Delta f}{fs} = \frac{C1}{2(CL + C0)} * 10^6 \quad (ppm) \quad (2)$$

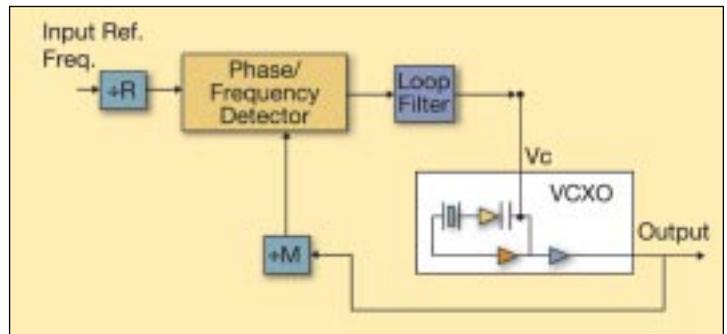Equation 2 gives you the distance in ppm from the series resonance

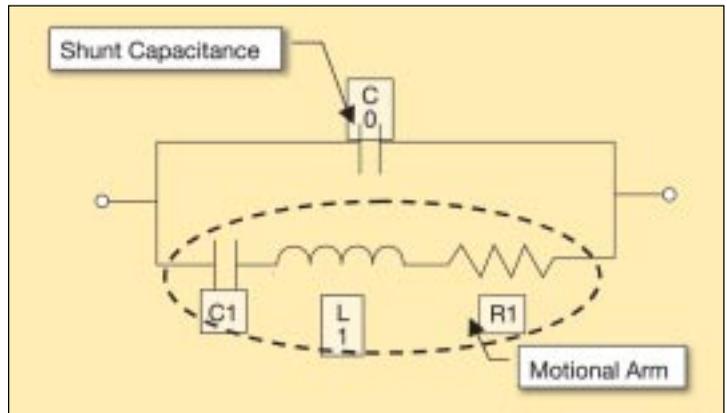**Figure 1. Basic PLL block diagram with VCXO.**

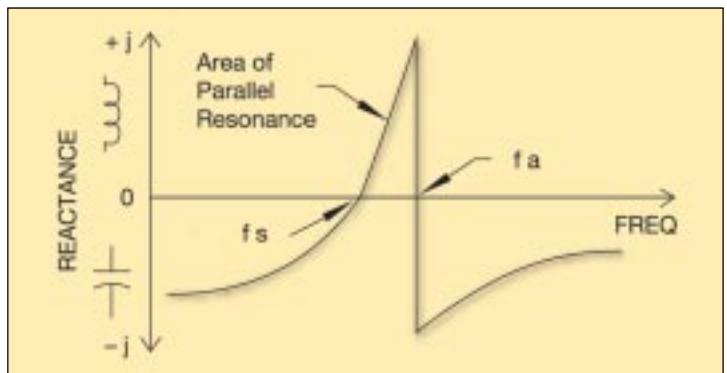**Figure 2. Single-mode, one-port, crystal resonator equivalent circuit model.**

Figure 3. Crystal's reactance curve.

point *fs*, to a certain load capacitance *CL*. The plot of Equation 2 is called the pulling curve of the crystal and is shown in Figure 4. From Equation 2 it can be seen that the larger *C1* is the greater the distance
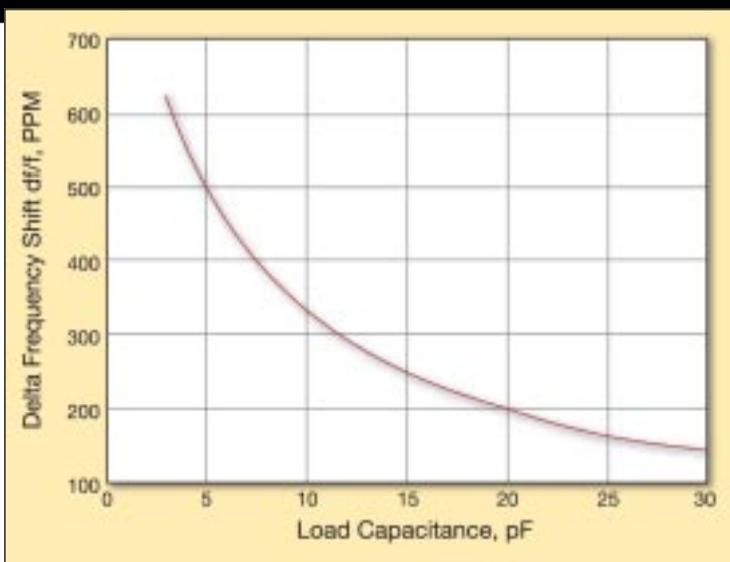
Figure 4. Pulling curve for a crystal with *C1*= 10 fF and *C0* = 5 pF as function of load capacitance.

from *fs* to a particular *CL* frequency (more pull). Thus, it is advantageous to have large *C1* values for a VCXO. Equation 2 also shows that *CL* and *C0* need to be specified as small as possible to maximize the pulling on the crystal. It turns out that *C1* is a function of *C0* and *C1* cannot be increased without increasing *C0*. Hence, once the *CL* value is selected, you need only specify the ratio of *C0/C1* as a certain maximum to complete the pulling specification requirement.

A more useful form of Equation 2 is the pulling equation from one load capacitance to another. That formula is:

$$Pull(CL1, CL2) = \frac{C1(CL2 - CL1)}{2(C0 + CL1)(C0 + CL2)} * 10^6 \quad (ppm) \quad (3)$$

The use of Equation 3 will be illustrated in the VCXO design example below.

VCXO design example

A 38.88 MHz VCXO will be used in a PLL application to synchronize to an input reference frequency that must remain locked for a minimum of 10 years. The operating temperature environment will be -10°C to +70°C. The input reference is known to have an overall accuracy of ± 20 ppm. Assume the internal VCXO circuitry has been designed to present a nominal load capacitance (C_{LN}) of 14 pF when the controlled voltage (Vc) is centered and 8 pF and 27 pF at low and high control voltage, respectively (C_{LL}, C_{LH}). Specify all the necessary crystal parameters for the VCXO.

Solution

Center Frequency: 38.88 MHz

Load Capacitance: 14pF

Mode of Operation: (For example, "fundamental" or "3rd overtone.") A crystal has multiple responses (see Figure 5). The first major response is called the fundamental. The next major response is the 3rd overtone, then the 5th and so on; only odds. Crystals have no harmonics, only overtones. Figure 2 can be expanded by adding an additional motional arm for each overtone response. The motional capacitance of the overtone arms will equal:

$$C_{Nth} = \frac{C1}{N^2} \quad (4)$$

where *N* is the overtone number and *C1* is the motional capacitance of the fundamental.

For example, the 3rd overtone motional capacitance is equal

to one-ninth the motional capacitance of the fundamental response. Because of this fact, it is difficult to pull an overtone crystal. Therefore, a pullable crystal is fundamental.

Resistance: Because the crystal is a passive component, it has losses that must be overcome by the oscillator circuit. It is the responsibility of the oscillator circuit designer or chip manufacturer to specify the maximum loss the crystal can have to guarantee reliable start-up under all conditions. If your circuit operates the crystal at *fs* or series point as in Figure 3, then the value of *R1* is the loss. But we are specifying a parallel and not a series crystal for this example because we already specified a load capacitance of 14 pF. So what is the loss, if it is not *R1*? In the area of parallel resonance the loss is a function of *CL* and *C0* and is given by:

$$E.S.R = R1(1 + C0/CL)^2 \quad (5)$$

where *E.S.R* stands for equivalent series resistance.

A good number to use for E.S.R is 50 Ω maximum.

Calibration or Tolerance: This is the frequency accuracy of the crystal at +25°C. The tighter you make this specification, the more the crystal will cost. Because we are tracking an input reference and the loop is always locked, the calibration number is not critical. A ± 25 ppm maximum figure will suffice.

Shunt Capacitance, C0: In modern crystals, this number is always 7 pF maximum. Alternately, it may be tied to the ratio of *C0/C1*.

Frequency Stability over Temperature: The crystal will vary over temperature, and a good number that will not incur cost is ± 30 ppm over -10°C to +70°C.

Aging: The crystal frequency will change over time. A good specification is ± 5 ppm first year, ± 2 ppm maximum per year thereafter.

Motional Capacitance, C1: To calculate the motional capacitance, we first need to figure out how much pulling will be required from the crystal. The minimum pulling required is:

minimum pull required = (input reference accuracy + total errors from crystal)

where the total errors from crystal = calibration + stability + aging for 10 years

= 25 + 30 + (5+18)

= ± 78 ppm

Therefore, minimum pull required

= 20 +78

= ± 98 ppm

Using Equation 3 and setting *C0* = 7pF, calculate a value of *C1*
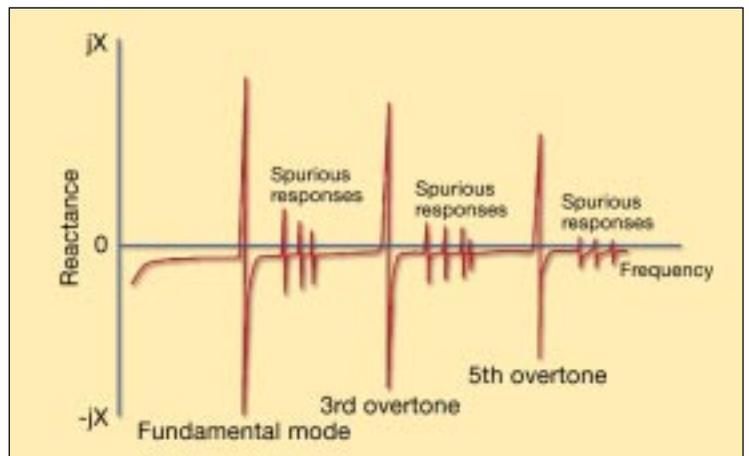

Figure 5. Crystal's responses.

The drive level should be measured in circuit to make sure the crystal is not being overdriven.

that will pull -98 ppm minimum from $C_{LN} = 14$ pF to $C_{LL} = 8$ pF. The same value of $C1$ must pull +98 ppm minimum from $C_{LN} = 14$ pF to $C_{LH} = 27$ pF. With $C1 = 11$ fF, we obtain a pull of = -104.8 ppm from 14 pF to 8 pF and +100.1 ppm from 14 pF to 27 pF. Therefore, $C1 = 11$ fF minimum and $C0 = 7$ pF maximum will meet the minimum pull required. Give yourself some extra margin and specify $C1 = 15$ fF minimum.

Cut of Crystal: (For example, AT-Cut or BT-Cut). The cut on a crystal refers to what angle(s) the crystal blank is cut. Angles of cut primarily affect the stability over temperature performance. Pullable crystals are made with AT-Cut quartz. A BT-Cut crystal has poor frequency vs. temperature stability in comparison with an AT-Cut. This extra error in frequency requires the VCXO to have much more pulling, which makes the BT-Cut undesirable as a pullable crystal. Therefore, specify AT-Cut.

Package or Holder Type: Many crystal packages are available to the designer. One way to go about it is to contact the crystal manufacturers with the specification already in hand, and they can help select the correct package. This is especially true for pullable crystals, which need to be in the larger packages due to large $C1$ values. For this example we chose a UM-1 package.

Drive Level: Drive level refers to how much RMS power the crystal can dissipate without breaking or experiencing excessive aging. The oscillator circuit designer or chip manufacturer should state the drive level the crystal sees in the circuit. The smaller the package, the lower the drive level specifiication will be. For the UM-1 package, a 500 uW maximum drive level specification is adequate. The drive level should be measured in circuit to make sure the crystal is not being overdriven.

There are other crystal specs, but below are the necessary specifications needed:

- ■ Frequency: 38.88 MHz
- ■ Mode: Fundamental
- ■ Load Cap: 14 pF
- ■ Calibration: ±25 ppm
- ■ Freq. Stability: ±30 ppm
- ■ Shunt Capacitance: 7 pF max.
- ■ Motional Capacitance: 15 fF min. or $C0/C1$ (7 pF/15 fF) = 466 max.
- ■ Aging: ±5 ppm 1st year, ±2 ppm per year thereafter
- ■ Quartz Cut: AT-Cut
- ■ Holder Type: UM-1
- ■ Drive Level: 500 uW max.

Thus, specifying a right pullable crystal in the design a VCXO will guarantee a PLL to synchronize, translate (up or down), and/or de-jitter an input reference frequency. **RFD**

ABOUT THE AUTHOR

Ramon M. Cerda, is director of engineering at Crystek Crystals Corp., Fort Myers, Fla. Cerda holds a BSEE (1985) and MSEE (1993) from Polytechnic University of New York. Before joining the crystals and oscillator field, he was an RF engineer for more than 10 years. Ramon can be reached via e-mail at rcerda@crystek.com.